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A—2—3 DESIGN LIMITATION DUE TO SUBSTRATE CURRENTS AND SECONDARY IMPACT IONIZATION ELECTRONS IN NMOS LSI'S

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Further advances in MOS LSI designs towards the reduction in device dimensions could cause a significant increase of the electric field. Impact ionization in the higher drain electric field results in more substantial substrate current, and the holes accelerated towards the substrate can originate the secondary impact ionization. It is well-known that the breakdown in short channel MOS transistors is in conjunction with the forward biasing of the source junction due to the substrate current, and authors have reported the minority carrier injection into the substrate during the transistor saturation operation and the resulting degradation of the device characteristics[1]. Therefore, the quantitative analysis of the substrate current including its secondary effects is very important for MOS LSI design considerations. In this paper, we describe a two-dimensional analysis of those effects and their experimental verifications. Design limitations are also discussed based on theoretical and experimental results.

A schematic diagram of an NMOS transistor illustrating the impact ionization currents is shown in Fig.1, and the dependences of the impact ionization rates on the effective channel length, junction depth and gate oxide thickness are shown in Fig.2. The reduction of the transistor dimensions results in a significant increase in the impact ionization rate. The two-dimensional numerical analysis, which gives accurate distributions of the electric field and the current, enabled us to obtain the impact ionization rate besides the drain current. As shown in Fig.3, the calculated values showed good agreement with the experimental results. With this model, substrate currents were accurately estimated for the first time.

The model of the minority carrier injection into the substrate is also shown in Fig.1. The generated holes flow to the substrate, and gain kinetic energies from the electric field in the depletion region. If they exceed impact ionization threshold, electron-hole pairs can be generated again. Due to the potential profile in this region, the electrons flow into the drain and the holes flow to the substrate. However, a fraction of the generated electrons near the deption edge can run into the substrate and then diffuse in the neutral bulk region. The measured spatial distribution of the injected electron current is shown in Fig.4 for various gate voltages. The excess electrons will decay by recombination process in the substrate, and the results in Fig.4 support the model with the diffusion length L_n=56μm. Fig.5 shows the substrate electron current at the position of the generation, as a function of the substrate hole current. The minority carrier injection ratio ($=I_{n,sx}/I_{sx}$) is about 4×10^{-5}, which is reasonably estimated by the calculation.

Based on our models and experimental results, limiting voltages for punch-through, parasitic bipolar breakdown, excess electrons and hot electron trapping are summarized in Fig.6. Impact

ionized excess electron limitation is determined as the carrier level exceeds the thermally generated electrons at the nearest neighbour. The result of a failure analysis of an actual LSI will be also presented.

1) J. Matsunaga and S. Kohyama: Appl. Phys. Lett. 33 (1978) 335

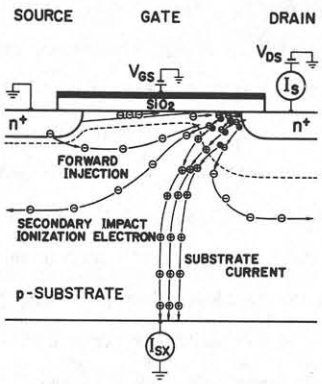

Fig.1 Schematic diagram illustrating substrate currents and secondary impact ionization electrons.

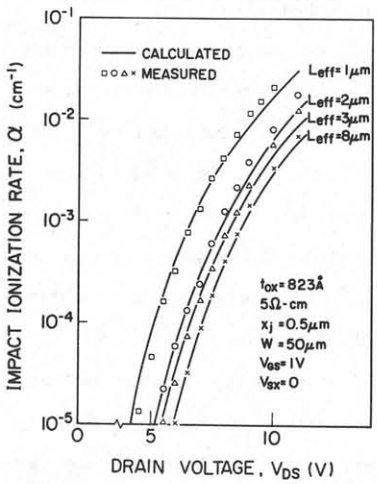

Fig.3 Measured and calculated impact ionization rates.

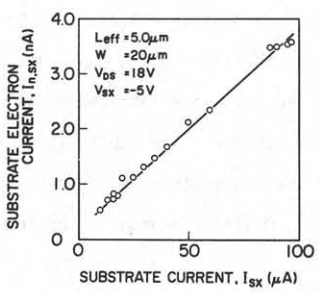

Fig.5 Substrate electron current as a function of the substrate current.

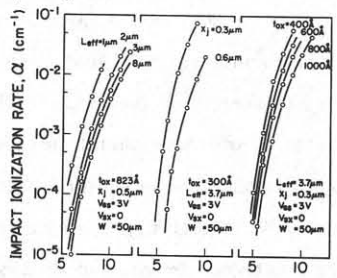

Fig.2 Drain voltage dependences of impact ionization rates for various transistor dimensions.

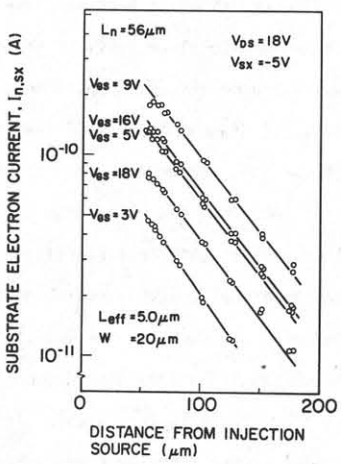

Fig.4 Substrate electron currents as a function of the distance from the generation source.

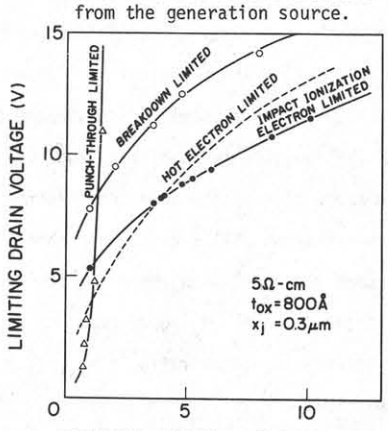

Fig.6 Limiting drain voltage as a function of the effective channel length.