B—1—2 MSI HIGH SPEED LOW POWER GaAs INTEGRATED CIRCUITS*

S. I. Long, B. M. Welch, R. C. Eden, F. S. Lee and R. Zucca

Rockwell International/Science Center
Thousand Oaks, California 91360

At the 1978 ISSCC, a new circuit approach to GaAs digital integrated circuits was presented.[1] This approach, which makes use of very small, high conductance, ultra low capacitance Schottky diodes for most logic functions, is referred to as Schottky Diode FET Logic (SDFL). Inversion and gain are obtained with low power depletion-mode MESFETs with 1μm gate lengths. In this paper, successful fabrication of circuits providing complex sequential and combinatorial logic functions is reported, including greater than 60 gate MSI circuits. These circuits are distinguished from previously published MSI GaAs IC results in that a) they are planar circuits fabricated by a multiple localized ion implantation process, b) very high gate densities (5×10^4 to $10^5/cm^2$) are possible, c) they contain larger numbers of gates and d) the gate power levels (~ 200μW to 2mW/gate are sufficiently low to allow achievement of LSI to VLSI complexity circuits. The logic propagation delays (τ_d ~ 100 ps) obtained are similar to those of previous depletion-mode GaAs FET IC's.[2]

Using the planar, SDFL approach, circuits in the MSI range of complexity have been designed, fabricated and tested. For example, binary ripple counters or frequency dividers have been made using the D flip-flop (DFF) as a basic building block. The DFF contains 6 NOR gates with maximum fanouts of 3. A three stage divider (divide-by-8) consisting of three T-connected DFF stages has been fabricated which contains 25 NOR gates. Clock frequencies up to 1.9GHz have been achieved on these DFF dividers which correspond to an equivalent gate propagation delay of 110ps. Dynamic switching energies of 0.3pJ/gate have been observed. In addition, power dissipations as low as 0.75mW/gate have been observed for DFF dividers fabricated on low pinchoff voltage wafers.

Larger MSI circuits including an 8 input data multiplexer containing 64 gates have been evaluated. This circuit utilizes a three stage, DFF implemented, synchronous counter as an address generator for the multiplexer gate array. The data output of the multiplexer is latched using another DFF stage to prevent glitching. Operation of this multiplexer has been achieved at a clock frequency of 1.12GHz. Power dissipation of the multiplexer circuits varied from 75mW to 375mW for wafers with pinchoff voltages of 0.5V and 1.45V, respectively.

A 1 input to 8 output data demultiplexer containing 60 gates was also fabricated and evaluated. The circuit design used for this device is quite similar to the data multiplexer. A synchronous counter provides the address for selecting 1 out of 8 NOR gates sharing a common data input. Operation of this circuit has been demonstrated at a clock frequency of 1.06GHz.

These initial results on depletion-mode GaAs MESFET IC's at the MSI level of complexity indicate that the high density, planar, SDFL circuit approach shows excellent promise for extension into high performance LSI logic circuits.

References

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