

C-2-4

Modified Schottky Barrier Heights
by Interfacial Doped Layers: MBE Al on GaAs

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We report here on progress in optimizing Schottky barrier heights using doped interfacial layers in Al:GaAs diodes grown in a molecular beam epitaxy (MBE) apparatus. It should be emphasized that these contacts were grown entirely in the ultra-high vacuum (UHV) environment of an MBE system, because this allowed us to minimize contamination and control the impurity content at the metal:semiconductor interface.

Schottky diodes are of significant technological importance because of their ease of fabrication and high speed. Their usefulness is limited, however, by the inflexibility of the barrier height: for many semiconductors the barrier height is relatively insensitive to the choice of metal. An early effort on Schottky barrier height modification involved Cu diffusion into n-type CdS¹. This was followed by an attempt using ion implantation of Sb into p-type Si². The use of doped interfacial layers to modify the barrier height was suggested independently for Schottky barriers on III-V semiconductors by W. E. Spicer et al. as a result of their detailed understanding of the process of Schottky barrier formation on these materials³.

In this study we have fabricated diodes on n-GaAs epitaxial layers ($n = 5 \times 10^{16} \text{ cm}^{-3}$) with Be-doped interfacial layers ($p = 10^{18} \text{ to } 10^{20} \text{ cm}^{-3}$) and epitaxial crystalline Al metal layers (Fig. 1). The GaAs and Al deposition conditions were chosen to yield the most abrupt, "ideal" interfaces. p^+ layer thicknesses, t , from 50 to 360 Å were investigated. The barrier heights, as determined by room temperature I-V measurements, extend from 0.79 eV for Al directly on n-GaAs surfaces, to heights greater than 1.1 eV utilizing a p^+ interfacial layer

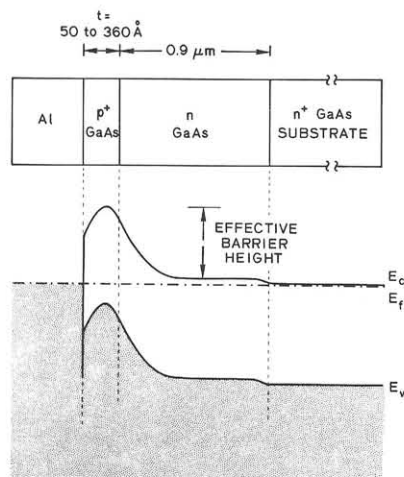


Figure 1. The metal- p^+ -n structure used for Schottky barrier height modification in this work, and the corresponding band diagram. The increased barrier height, resulting from the negative space charge in the fully depleted p^+ region, is shown.

(Fig. 2). The ideality factors, n , of these diodes were 1.04 to 1.21. Some increase of n above unity is expected for these structures. The observed increase will be compared with theory.

Our theoretical calculation of the barrier height is an improvement upon that of previous workers, and utilizes an understanding afforded by our unified defect model for interface states on III-V semiconductors³. The unified model gives detailed insight into the energies and densities of the (defect-induced) interface states that pin the Fermi level. We find good agreement between theory and experiment (Fig. 2). A full calculation of the electrostatics at the interface is under way, but it is evident that the Schottky barrier height on GaAs can be engineered to any desired value over a much broader range than previously thought.

I-V, C-V, internal photoemission, and temperature-dependent measurements have been made. These results were interpreted in conjunction with model charge distributions and electric potentials, and known doping configurations to lend insight to phenomena at metal:semiconductor junctions.

The advantages resulting from engineered Schottky barriers include lower gate currents and reduced noise in GaAs MESFET's, improved performance in solar cell applications, as well as increased flexibility in circuit design with diodes of differing barrier heights. Schottky diodes can be fabricated having large barrier heights approaching those of p-n junctions. Since these are majority carrier devices they should not suffer from the minority carrier charge storage problems which limit the speed of bipolar devices. Diodes can be fabricated that range continuously from majority carrier Schottky devices to recombination dominated p-n junctions. These devices should also facilitate the study of transport mechanisms at rectifying contacts.

Supported in part by ARPA no. N00014-79-C-0072 through ONR, and ONR no. N00014-75-C-0289.

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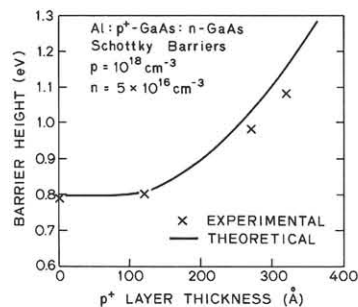


Figure 2. Effective barrier heights, calculated from room temperature I-V measurements assuming a thermionic emission model, for some diodes having the structure shown in Fig. 1. The solid line shows the predictions of our model.