Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 193-196

Electrical Properties of Surface Defects on Molecular Beam Epitaxially Grown GaAs Layers and Defect Free Growth Procedures

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Electrical properties of oval defects including effects of these defects on MES-FETs are investigated and defect-free growth procedures are presented. Oval defect cores have higher densities of recombination centers than the normal epi-layers. Oval defects are regarded as non-active regions due to extremely low carrier density, so that the defects decrease FET transconductance. Eliminating oxygen in the Ga source and growth environment reduces the defect density to less than $5\times10^2/cm^2$.

§ 1. Introduction

Molecular beam epitaxy (MBE) is a potential epitaxial growth technique for fabricating optical and electronic devices. However, it has not been a viable method for fabricating integrated circuits because its use results in a great number of surface defects called oval defects. The crystallographical structure and origin of these defects have been studied intensively and attempts have been made to eliminate the defects.[1-5] These reports have shown that oval defects include stacking faults and inferior crystal quality. As for defect origin, Ga spitting from the Ga melt,[2] Ga oxide in the Ga melt,[3] and As particles,[4] have all been suggested. However, the actual mechanism is still uncertain and to date the defects have not yet been eliminated completely. Moreover, despite their high density, $\sim 10^5/cm^2$, and large size, 10-50 μm^2, the effects of oval defects and their electrical properties on optical and electronic device performance have not been fully investigated.

The authors previously studied the mechanisms of oval defect formation and determined that Ga droplets were responsible for oval defect formation where the droplets might be formed by the dissociation of Ga oxides on the Ga melt source in an usual growth rate range (0.4 - 3 μm/hr).[6] A study of the electrical properties of oval defects found that these defects have high resistivity characteristics.[7]

This paper describes the electrical properties of oval defects which are closely related to the crystalline structures of the defect core and the hillock surrounding the core. Also, growth procedures for realizing almost defect-free epi-layers are proposed.

§ 2. Experiments

Epitaxial growth was performed using a RIBER 2300P system which makes it possible to grow successive GaAs layers under identical conditions. The substrate crystals were Cr-doped or undoped semi-insulating LEC GaAs. Electron beam induced current (EBIC) technique was employed to study the electrical properties of oval defects in 1 μm thick Si doped (10^{16}-10^{17} $/cm^3$) GaAs layers. The EBIC image was obtained by injecting electron beams at 20 keV through a 500 Å-thick Au-Ge alloy Shottky contact. The electron penetration depth in the GaAs layer was deeper than the depletion layer.

Two types of MES-FETs with gate lengths of 2 or 4 μm and a gate width of 20 μm were fabricated on a 0.1 μm thick Si doped (1×10^{17} $/cm^3$) GaAs epi-layer grown on a 1.5 μm thick undoped GaAs buffer layer at 650 °C. The separation between the gate and the source/or the drain was 2 μm.

§ 3. Results and discussion

3.1 Electrical properties of oval defects

A typical oval defect consisted of a core and a hillock surrounding the core. In a previous paper,[7] the recombination centers in oval defects were analized using the EBIC observations of the top surface of the defects. In this paper, a more detailed EBIC observation of the oval defect cross section was performed as shown in Fig.1. The dark area in the oval defect image corresponds to a lower induced current and coincides with the core. This shows that many recombination centers are included in the core. Moreover, it should be emphasized that the bottom of the core appears to be dark. This strongly suggests that the cores have been anomalously formed on a small nucleus adhered to the GaAs surface prior to or during the epi-layer growth. On the other hand, the image of the hillock region is light, as has been reported.[7] The result can be explained as follows: Since the higher induced current has been collected, one possibility is straightforward, i.e., the hillock region would have fewer recombination centers. Another possibility to be considered is that the depletion layer under the hillock would be thicker. In other words, carrier concentration of the hillock region is lower than that of the normal epi-layer, as will be shown later. This indicates that the volume where EBIC is collected should be larger in the hillock region than that in the normal layer, which results in light image formation. In this case, the density of recombination center might not be low in the hillock region. We can not exclude either possibility right now. Further study is in progress.

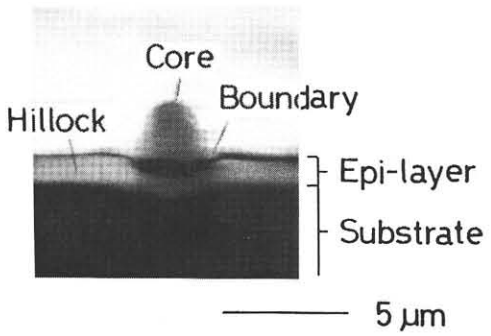

Fig.1 Electron beam induced current image of oval defect cross section.

The effects of oval defects on such FET properties as source-drain conductance and gate breakdown voltage have already been discussed.[7] It has shown that despite their high resistivity characteristics, oval defects decrease gate breakdown voltages only when their cores are located at gate edges. In this paper, the effect of oval defects on transconductance g_m, which is one of the representative parameters in FET performance, are investigated as shown in Fig.2. Here, g_{mov} is the transconductance for the case where oval defects exist between the source and the drain, g_{mf} is the transconductance under defect-free conditions, S_{sd} is the area between the source and the drain ($6 \times 20\ \mu m^2$) and S_{ov} is the microscopically determined area occupied by oval defects in S_{sd}. The g_m value was compared at the source drain voltage V_{sd}=1V and the gate voltage V_g= 0.55V. A decrease in g_m, as a result of increasing the oval defect occupation ratio, is caused by the high resistivity of the oval defects.

In order to clarify the cause of this characteristic, carrier density in the oval defect was investigated as shown in Fig.3. N_{ov} is the averaged carrier density in the GaAs layer with

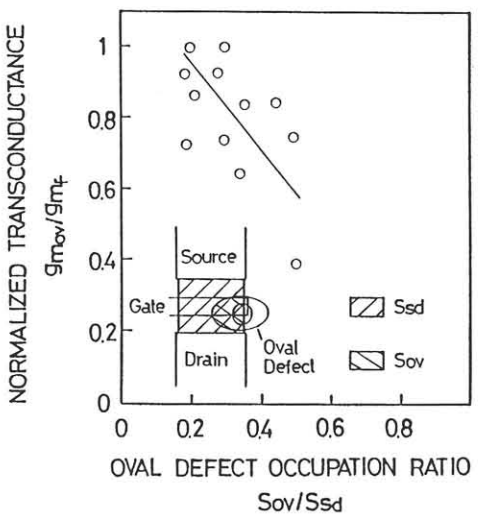

Fig.2 Normalized transconductance as a function of oval defect occupation ratio in the source-to-drain area.

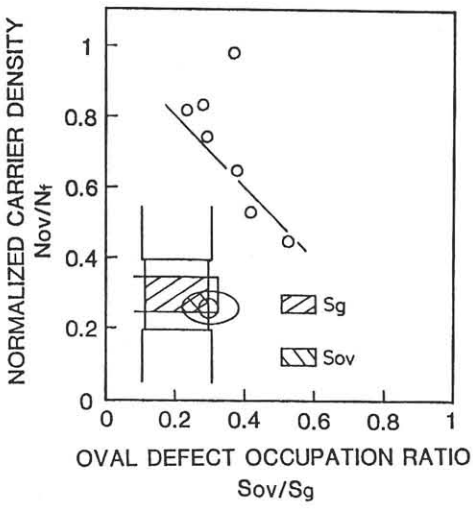

Fig.3 Normalized carrier density as a function of oval defect occupation ratio in the gate area.

oval defects under the gate pattern, N_f is for defect free conditions and S_{ov} is the microscopically determined area occupied by the oval defects in S_g which is the gate area (4x20 μm^2). These carrier densities were estimated by C-V measurements, when a forward voltage of less than 0.6 V was applied to the gate and the source was used as an ohmic electrode. Carrier density in the oval defects is seen to be negligible compared with a normal epi-layer by a very low N_{ov}/N_f value when the experimentally determined line in Fig.3 is extrapolated to $S_{ov}/S_g = 1$. That is, the oval defect is regarded as a non-active region. This extremely low carrier density is due to the relatively low doping concentration resulting from a higher growth rate for oval defects than that for normal epi-layers.

3.2 Origin of oval defects and defect-free procedures

Variations in oval defect density related to such growth parameters as growth rate, substrate temparature and As/Ga flux ratio have been systematically investigated for equi-thickness epi-layer samples. Increases in density from $10^3/cm^2$ to $10^5/cm^2$ have been noticeably observed as a result of increasing the growth rate from 0.4 μm/hr to 6 μm/hr, while the other parameters were held constant. These results were analized thermodynamically and a consistent relationship was obtained between the defect density and Ga oxide formation on the Ga melt source in a rather low growth rate region (0.4 - 3 μm/hr), and Ga droplets in a high growth rate region (4 - 6 μm/hr).[6)]

It was also assumed that Ga droplet formation in the Ga cell might be triggered by Ga oxide dissociation under usual growth rate conditions (0.5-1 μm/hr) for electronic devices when the cell orifice shutter was opened to initiate the growth, so that the Ga droplets arriving at and adhering to the GaAs substrate were the source of the oval defects. Although it is very difficult to confirm Ga oxide formation on the Ga melt source during the shutter-closed condition, some experimental results indirectly support this assumption. When the shutter was closed intermittently for 1 hour between two 30 minutes growths, the oval defect density was about 60 % greater than in layers grown continuously for 1 hour at the same growth rate. This supports the idea that the density of oval defects in the low growth rate range is primarily determined in the initial stages of epitaxial growth just after the shutter is opened.

On the other hand, in the high growth rate range, it is believed that Ga droplets or spitting, which occur spontaneously in a high temperature Ga cell, are the main cause of oval defects formation. This result in the high growth rate range can be deduced from the following observations: 1) Not only the oval defect density but also defect size depended on GaAs layer thickness. 2) When GaAs was grown at 960°C (1.3 μm/hr) after the Ga source was once pre-heated at 1150°C (5.3 μm/hr) and rapidly cooled, the surface morphology of the epi-layer was deteriorated by many hillocks/or small size oval defects (see Fig.4) which were very similar to those observed for epi-layers grown at high growth rates. This deteriorated morphology was not observed for epi-layers grown at 960°C without pre-heating treatment.

These results indicate that to obtain GaAs layers ($< 500/cm^2$) which are almost free from defects it is necessary to reduce the growth rate to less than 0.4 μm/hr or to protect

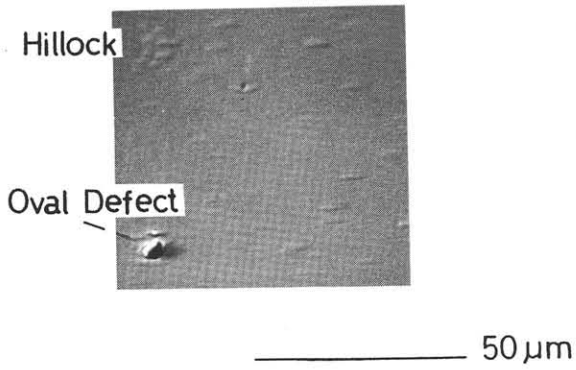

Fig.4 Scanning electron micrograph of GaAs surface morphology.

the Ga source from oxidation. In order to obtain defect-free GaAs layers at a practical growth rate of 1 μm/hr, some procedures for preventing Ga source oxidation were investigated and the following were found to be effective. 1) long-time chamber baking (> 72 hours). 2) Ga cell pre-heating to about 1200°C under shutter-opened condition just after charging the Ga source. 3) charging the Ga source in dry N_2 atmosphere. It is noted that the oval defect density could be reduced to about 1/10 the present level at the same growth rate of 1 μm/hr by executing these procedures as shown in Fig.5.

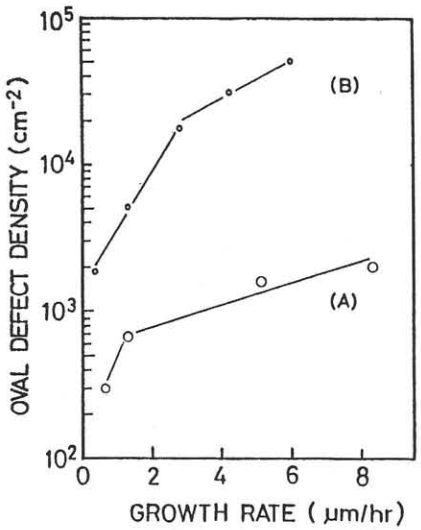

Fig.5 Oval defect density as a funtion of growth rate. (A) With defect free procedures. (B) Without defect free procedures.

§ 4. Conclusions

1. Oval defects consist of a core and a hillock surrounding the core. The core, which includes high density of recombination centers, seems to originate from a droplet adhered prior to or during the growth.

2. Oval defects, which have high resistivity characteristics due to lower carrier density than the normal epi-layer, decrease FET transconductance.

3. The most effective growth procedure for eliminating oval defects is the prevention of Ga oxide formation on the Ga melt source, which may trigger the creation of Ga droplets resulting in nucleus generation in the oval defect core.

Acknowledgements

The authors would like to thank Mr.Hiroaki Takeuchi in our labolatory for his technical assistance in the MBE growth.

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