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Effect of Trap-State on Field-Effect Mobility of MOSFET's Formed on Large Grain Poly-Si Films

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Electrical characteristics of large-grain polysilicon transistors were presented for various grain sizes. The field-effect mobilities of poly-Si transistors were studied based on thermionic emission model with potential barrier at grain boundaries. Electron mobility within the grains were evaluated to be 194 $cm^2/V.s$. Our result indicates that, using the electron mobility within the grains, thermionic emission model can be applicable to the poly-Si films with fairly large grain size.

1. INTRODUCTION

In higher packing density of VLSI, poly-crystalline-silicon (poly-Si) transistors fabricated on insulating substrates have been of great interest due to their usefulness for a formation of stacked devices[1-3]. In poly-Si transistors, grain boundaries exert a profound influence on device characteristics because the large number of electronic charges trapped at grain boundaries form potential barriers, which deteriorate carrier transport in poly-Si[4)5)]. This thermionic emission model has been developed for fine-grain poly-Si films.

Recently, in order to improve device characteristics, the use of large-grain poly-Si were demonstrated[6)7)]. However, it has been not yet clarified whether this model can be applicable to these large grain poly-Si films.

This report investigates the effect of trap states on device characteristics using poly-Si films prepared by different crystallization process. The grain sizes of these poly-Si films ranged from 0.1 μm to 3 μm. Using these various poly-Si films, field-effect mobility of poly-Si MOSFET's is also analyzed based on the thermionic emission model.

2. EXPERIMENTAL PROCEDURE

Large-grain poly-Si films on SiO_2/Si substrates were formed by solid-phase crystallization of amorphous-silicon (a-Si), which were prepared by three different techniques: 1) Si implantation into LPCVD poly-Si, 2) APCVD, 3) LPCVD. Conventional LPCVD poly-Si films were also prepared for comparison.

Silicon-oxides were grown to 600-nm thick on 4-inch Si substrates. Then, amorphous-Si or poly-Si film of 150 nm thickness was deposited. Deposition temperatures were 620°C for LPCVD poly-Si film, 550°C for APCVD a-Si film, and 550°C for LPCVD a-Si film. Some of LPCVD poly-Si films were implanted by Si ions with acceleration voltages of 100 and 150 KV to be transformed into a-Si. These a-Si films were crystallized by annealing at 600°C in nitrogen. In Fig.1, grain sizes as a function of annealing time, which were estimated by TEM observation, were shown. Average grain size in each film after 16-hour annealing was 2-3 μm for a-Si formed by Si implantation, 0.4-0.7 μm for APCVD a-Si, 0.3-0.6 μm for

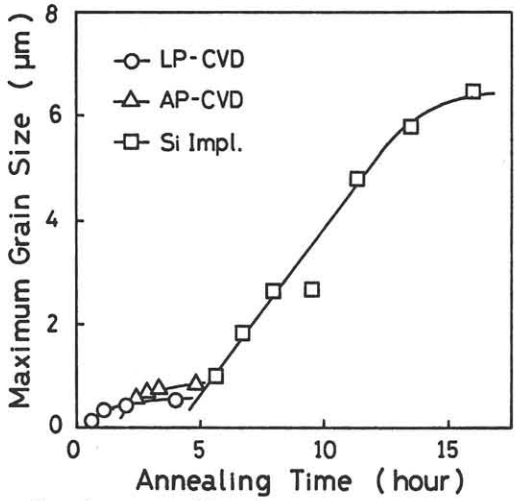

Fig.1. Grain growth of amorphous deposited film as a function of annealing time at 600°C.

LPCVD a-Si. The grain size of LPCVD poly-Si was about 0.1 μm. Although large grain sizes were attained, TEM observation revealed out that there were many defects, such as micro-twins, in each grains[7].

Poly-Si transistors were fabricated on large grain poly-Si films by conventional Si-gate process. After isolation of poly-Si films, a gate oxide was grown to a thickness of 38 nm in dry oxygen. Source and drain regions were formed by phosphorus ion implantation and subsequent annealing at 850°C. After final passivation with plasma silicon-nitride film, a part of the devices were annealed at 450°C for 60 min in H_2 for hydrogen passivation of grain boundaries.

The transistors measured have a channel width of 8 um, and a channel length of 10 um in a mask size. According to enhanced dopant diffusion along grain boundaries, an effective channel length became small to 7-8 um. This diffusion length is different for grain sizes and become large when grain size is small.

3. RESULTS AND DISCUSSION

Figure 2 shows typical subthreshold characteristics of poly-Si transistors. Electrical characteristics are improved with large grain poly-Si films, and also by hydrogenation. Although leakage current levels are almost the same, ON-state current depends strongly on grain size and hydrogenation. Maximum electron mobility of 110 $cm^2/V.s$ was obtained in Si implanted sample. The reason of this improvement is discussed as follows.

In poly-Si films, there are numerous crystalline defects at grain boundaries. These defects trap carriers, become charged, and lead to form potential barriers. According to the thermionic emission model, a drain current at a linear region is given as follows,

$$I_d = u_b \cdot (1/C_i) \cdot (W/L) \cdot \exp(-\phi_b/kT). \quad (1)$$

Therefore, barrier height can be estimated by measuring temperature-dependence of drain currents.

Figure 3 shows the activation energy for various samples as a function of gate voltage. The activation energy is around 0.6 eV, close to E_g / 2, where V_g is below threshold voltage V_t. This is an indication of complete grain depletion. When the gate voltage is increasing, the activation energy falls with increasing carrier density. These values fall more rapidly for poly-Si films of large grain size and/or hydrogenation anneal. According to Seto's theory[4], the potential barrier height can be expressed by

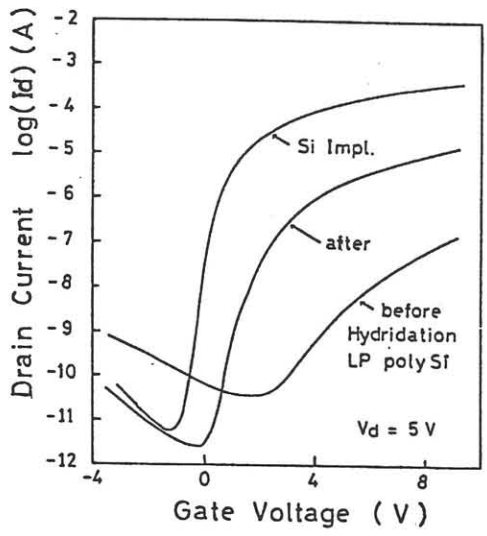

Fig.2. Subthreshold characteristics of poly-Si transistors at V_d = 5V.

$$\phi_b = (q\ N_{st}^2/8\varepsilon n), \qquad (2)$$

where N_{st} is a trap state density at grain boundaries, and n is a average carrier concentration . In MOSFET system, the carrier concentration in the inversion layer is simply given by

$$n = C_i/q \cdot d_{ch} \cdot (V_g - V_t) = K\ (V_g - V_t), \qquad (3)$$

where C_i is gate capacitance, d_{ch} is inversion layer thickness, thus K is a constant. The value of K was calculated to be 9.9×10^{18} ($cm^{-3}V^{-1}$), where the donor concentration was 1.0×10^{16} cm^{-3} and the gate oxide thickness was 38 nm. A threshold voltage V_t in Eq.(1) was estimated to be -0.2 V. Hence the potential barrier is expressed by

$$\phi_b = (\ q\ N_{st}^2/8\varepsilon K(V_g - V_t)). \qquad (4)$$

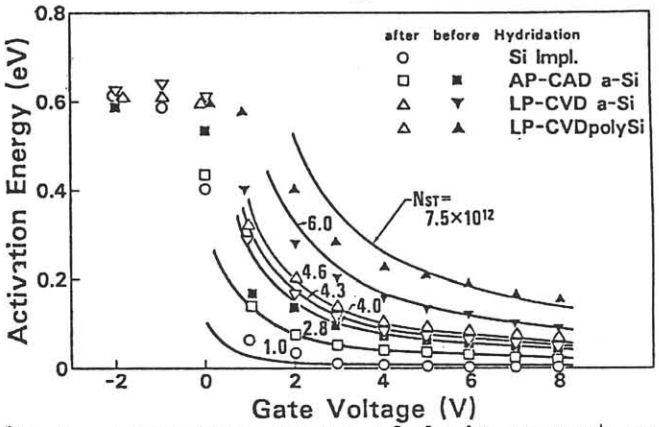

Fig.3. Activation energy of drain current as a function of gate voltage. Solid lines are calculated with Seto's theory.

N_{st} can be obtained by comparing measured values in Fig.3 and calculated values with Eq.(2). It is noted that calculations need only two parameters, n and Vt. The calculated value N_{st} is summarized in Table I. The N_{st} becomes small as a grain size is large, in other word, the number of grain boundaries in the channel region is small. In Si-implanted samples, N_{st} is below 1×10^{12} cm^{-2} and the effect of potential barrier is almost negligible. Nst is also reduced to two-third by hydrogenation using P-SiN.

Carrier mobility ue in a linear region is given from Eq.(1) and (4),

$$\mu_e = \mu_0\ (1 + q^2\ N_{st}^2\ /8\varepsilon \cdot kT \cdot K(V_g - V_t))$$
$$\times \exp(-\ q^2\ N_{st}^2\ /8\varepsilon\ kT \cdot K(V_g - V_t)) \qquad (5)$$

Table I. Summary of trap-state densities and field-effect mobilities of poly-Si transistors.

Sample		LP-poly	LP a-Si	AP a-Si	Si Impl.
Grain Size (μm)		≈0.1	0.3-0.6	0.4-0.7	2-3
Hydridation before	N_{st} (cm^{-2})	7.5E12	6.0E12	4.0E12	
	μ_{fe}(cm^2/V.s)	0.030	1.41	19.3	
Hydridation after	N_{st} (cm^{-2})	4.6E12	4.3E12	2.8E12	<1E12
	μ_{fe}(cm^2/V.s)	0.41	22	41	85

where barrier height is a function of N_{st} and V_g as shown in Eq. (1), and Eq. (2). Carrier mobility is given by only N_{st}, V_g, and u_0.

In addition, the effect of vertical electric field is taken into consideration as this formula,

$$\mu_{eff} = \mu_e\ /\ (1+E_{eff}/E_{crit})\ . \qquad (6)$$

Figure 4 shows μ_{eff} as a function of N_{st} at V_g = 5 V. Solid line indicates best-fitted curve to the measured points. The carrier density evaluated from this line is close to the calculated value at V_g = 5V, which indicates the discussion above is reasonable.

Pre-exponential term, u_0 = 194 cm^2/V.s would be the value where N_{st} = 0, in other words, there is no grain boundary in the channel region, which means that it is the

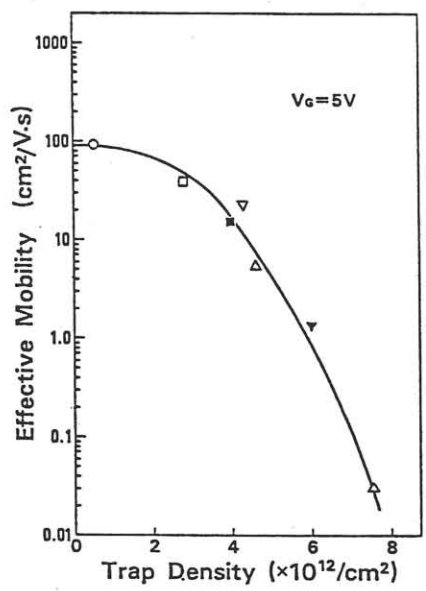

Fig.4. Relationship between field-effect mobility and grain-boundary trap-state density at V_g = 5 V.

carrier mobility within each grains. This value, 194 $cm^2/V.s$, is almost the same as the field-effect mobility, 165 $cm^2/V.s$, for electrons of grain-boundary-free poly-Si MOSFET's[7], and is also close to the value, 170 cm2/V.s, which is given for the twinned-region in the Si L-SPE layers[8]. These results indicate that crystalline defects in each poly-Si grain also limit the maximum carrier mobility in poly-Si films.

Measured values of carrier mobility, μ_{eff}, for each samples are given in FIg. 5. Calculated vaules with μ_0, N_{st}, and E_{crit}, as a parameter of V_g are also shown in Fig. 5 and represent a good agreement with calculated values.

Thermionic emission model with potential barrier at grain boundaries has been developed for poly-Si transistors, but it assumes that grain size of poly-Si is much smaller than channel length. In our sample, Si-implanted crystallized poly-Si has a large grain size of 2-3 um, and the channel length of poly-Si transistors we made is about 8 um. Therefore the number of grain boundary in the channel region is estimated to be 3 to 5. However, even in a small number of grain boundaries, the electrical characteristics experimentally obtained show good agreement with thermionic emission model, which indicate that it can be applicable to the poly-Si with fairly large grain size.

4. CONCLUSIONS

The relationship between field-effect mobility and trap-state density in poly-Si transistors are analyzed based on thermionic emission model. For this study, transistors were formed on large-grain poly-Si prepared by three different crystallization techniques. An electron mobility in the poly-Si grain was estimated to be 194 $cm^2/V.s$ and was close to that in the twinned region in Si L-SPE layers.

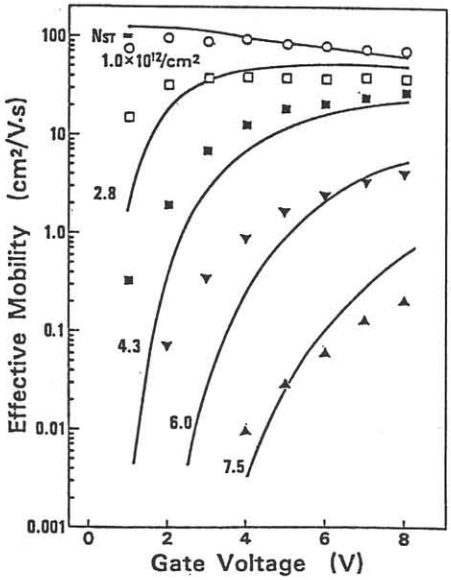

Fig.5. Electron mobility as a parameter of gate voltage. Solid lines indicate calculated value with V_g, N_{st}, and E_{crit}.

The field-effect mobilities are compared with thermionic emission model with potential barrier at grain boundaries and presented a good agreement, which indicates that thermionic emission model is successfully applicable to fairly large grain poly-Si. It has been clarified that the mobility in poly-Si grain μ_g and the trap state density N_{st} are two main factors necessary to predict field-effect mobility in poly-Si transistors.

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