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Capacitance-Enhanced Stacked-Capacitor with Engraved Storage Electrode for Deep Submicron DRAMs

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A technology has been developed for engraving storage electrodes to enhance the storage capacitance in DRAM, using a resist / SOG mixture. A large capacitance twice more than that of the conventional method is obtained by controlling resist particle size and poly-Si etching-time at an engraving process. The resist particle size is controlled by (1) resist/SOG mixing ratio, and (2) thickness of the mixture coated on poly-Si storage electrodes.

A SiO_2/Si_3N_4 composite film shows excellent reliability even on the engraved storage electrode.

INTRODUCTION

In megabit-class DRAMs, three-dimensional memory cell structures are necessary to get sufficient storage capacitance in a limited area. A stacked capacitor cell is one of the most promising candidates [1] [2]. However, for future DRAMs, storage capacitance must be enhanced even more. One approach to meet this requirement is to reduce the effective thickness of capacitor insulator films. Many studies have been reported so far on this approach. Most of them adopt new materials such as Ta_2O_5 [3].

However, the purpose of this work is to propose a technique for enhancing the storage capacitance without reducing the capacitor film thickness.

PROCESS STEPS FOR ENGRAVED STORAGE ELECTRODE

Key fabrication steps are described in Fig. 1. (a) First, 600nm-thick poly-Si is deposited on a selectively oxidized n-type Si substrate by low pressure chemical vapor deposition (LPCVD). After a phosphorus diffusion utilizing $POCl_3$ source, a mixture of spin-on-glass (SOG) and resist is coated on the poly-Si. In this mixture, fine particles of resist are suspended in the SOG because of a larger surface tension. (b) After the mixed film is baked at 160℃, the SOG is selectively etched in a buffered HF solution, leaving only the resist particles on the poly-Si. Figure 2 shows an SEM of the resist particles. (c) The poly-Si is etched by dry-etching utilizing dispersed resist particles as an etching-mask. After the resist particles are removed, the poly-Si is patterned to form storage electrodes. An SEM of the storage electrodes thus fabricated is shown in Fig. 3.

In order to investigate the electrical characteristics of a stacked capacitor having the engraved storage electrode, the poly-Si/insulator/poly-Si capacitors are fabricated as shown in Fig. 1. (d). We mainly adopt 5nm-thick SiO_2/Si_3N_4 composite film as a capacitor insulator [4].

The SiO_2 equivalent film thickness of the composite film, d_{eff}, is calculated from the capacitance, adopting 3.82 as a relative dielectric constant. The electric field applied to the capacitor is normalized by the d_{eff}.

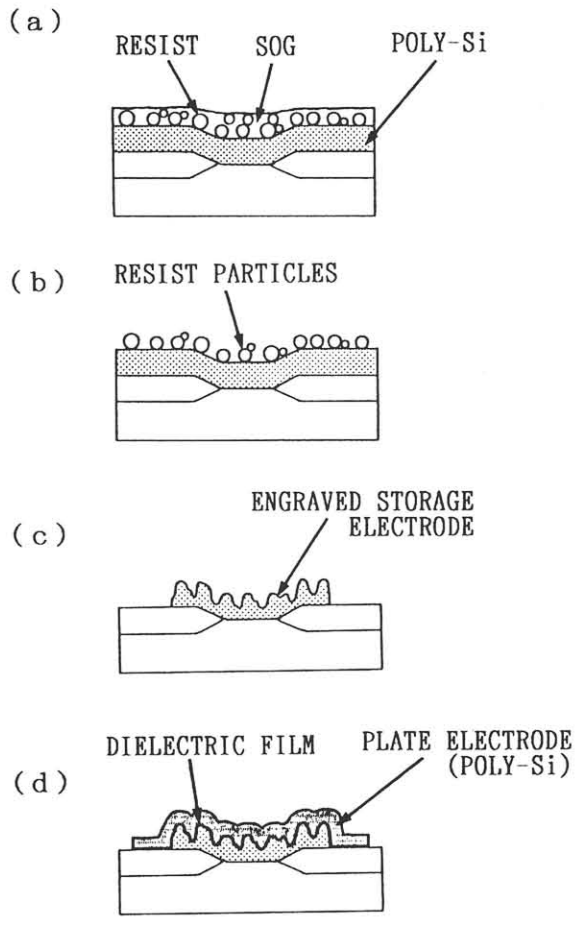


Fig.1 Key fabrication steps for a capacitor with an engraved storage electrode

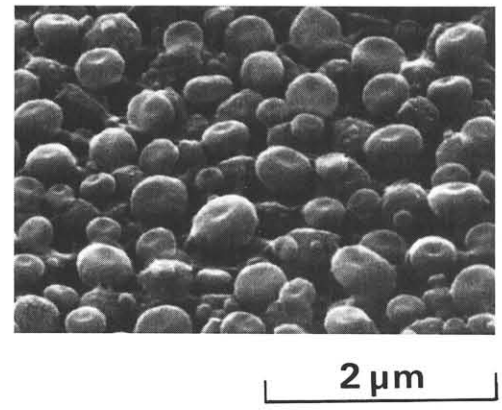


Fig.2 SEM photograph of resist particles

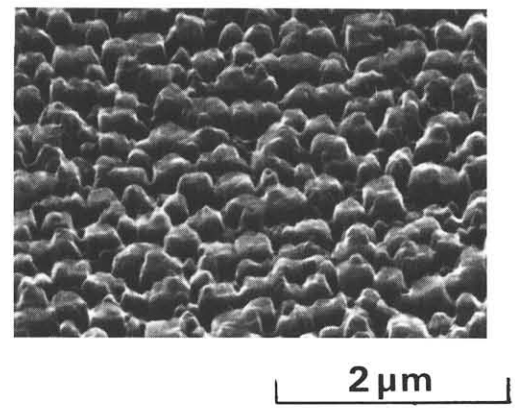


Fig.3 SEM photograph of engraved storage electrodes before patterning

ENHANCEMENT OF STORAGE CAPACITANCE WITH ENGRAVED STORAGE ELECTRODE

Figure 4 shows the capacitance of the stacked capacitors having the engraved electrode as a function of poly-Si etching-time during engraving process (Fig.1(b)~(c)). The 0.54 μm-thick resist/SOG mixture was coated in this experiment. The capacitance increases linearly with etching-time. Capacitance enhancement is remarkable for a small resist/SOG mixing ratio, which results from fine resist particles. A larger capacitance is also obtained for a thinner mixture film, which is also a result of small resist particles. Thus, by controlling resist particle size and etching-time, the capacitance can be increased to more than twice as that of a conventional stacked capacitor (no poly-Si engraving).

RELIABILITY OF CAPACITOR INSULATOR

1. I-V CHARACTERISTICS

Figure 5 shows I-V characteristics of capacitor insulators formed on the engraved storage electrode and on a conventional one. In this experiment, we used LPCVD-SiO_2 film (Fig.5(a)) and SiO_2/Si_3N_4 composite film(Fig.5(b)) as a capacitor insulator. The plate electrode was positively biased with respect to the storage electrode. The projected capacitor area was $5\times10^{-3}cm^2$. As is shown in Fig.5(a), the leakage current through the LPCVD-SiO_2 film increases markedly for the engraved storage electrode in comparison with that for the conventional one. On the other hand, the SiO_2/Si_3N_4 film shows no such a large increase (Fig.5(b)). Only slight a difference is found between the two types of electrodes at a high electric field.

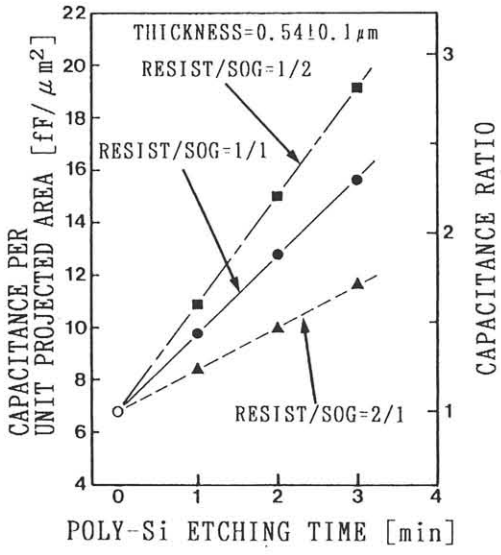
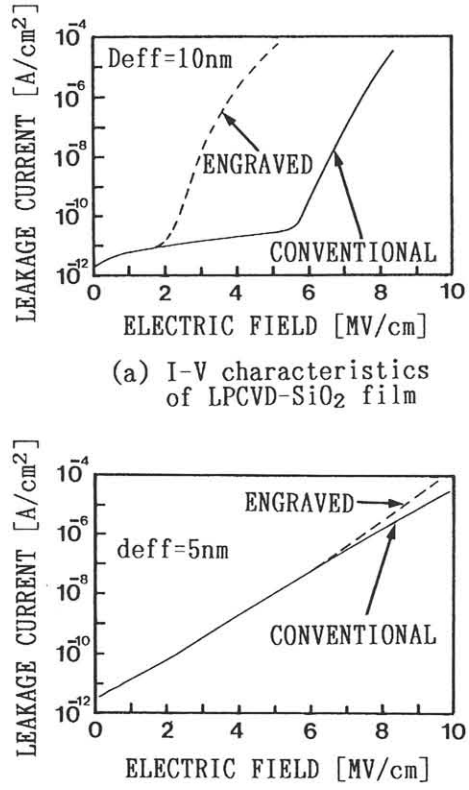


Fig. 4 Capacitance per unit projected area versus poly-Si etching time

Figure 6 shows distributions of critical field, Ec, both for an engraved storage electrode and for a conventional one. Here, Ec is the electric field corresponding to a 10^{-6} A/cm^2 leakage current. The capacitor insulator used is SiO_2/Si_3N_4 film. It should be noted that the distribution of Ec for the engraved storage electrode is quite similar to that for the conventional one.

We consider that the above results are due to the locally enhanced electric field in the film. It is explained in the following. There are two factors which bring about the field enhancement. One is sharp edges in the underlying substrate, especially those in engraved electrodes. The other is the thinning of LPCVD films at the side of substrate steps.

According to our experiments, the thinning of LPCVD -SiO_2 films is more remarkable, compared with LPCVD-Si_3N_4 films, leading to a more enhancement in the electric field. Moreover, the leakage current through the LPCVD -SiO_2 films follows Fowler -Nordheim process which is very sensitive to an electric field variation. As a result, the leakage current becomes larger for the engraved electrode.



(a) I-V characteristics of LPCVD-SiO_2 film

(b) I-V characteristics of SiO_2/Si_3N_4 composite film

Fig. 5 I-V Characteristics, of capacitor insulators on an engraved storage electrode and on a conventional one

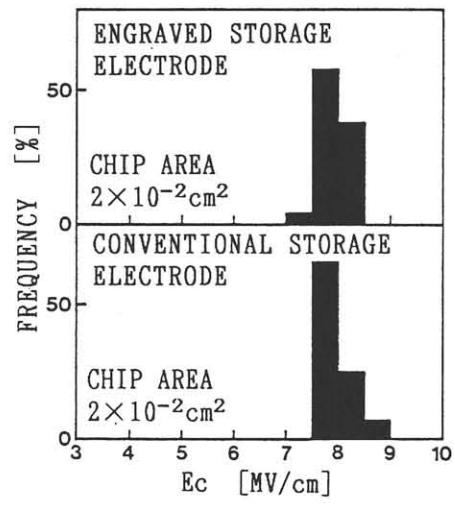


Fig. 6 Distribution of critical fields, comparison between engraved storage electrode and conventional storage electrode

On the other hand, the LPCVD-Si_3N_4 film has a better step coverage, and it is almost free from the field enhancement resulting from the thinning. The leakage current through the SiO_2/Si_3N_4 film is limited by Poole-Frenkel process which is not so sensitive to the electric field [4]. These facts lead to a slight increase in the leakage current for the engraved electrode.

2. TDDB CHARACTERISTICS

The time-to-breakdown of capacitors with engraved storage electrodes was measured by stressing capacitors having $10^{-6}cm^2$ projected area. The result is shown in Fig.7. The time-to-breakdown of the SiO_2/Si_3N_4 composite films is sufficiently long reaching 10^{18} sec for a conventional electrode, and 10^{17} sec for an engraved electrode, under a normal operation condition (3MV / cm). This difference in the time-to-breakdown is negligible in DRAM applications, because the lifetime required of DRAMs is 10 years (3×10^8 sec).

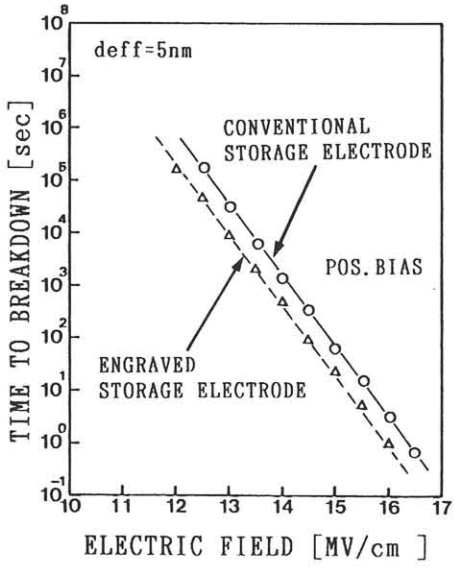


Fig.7 Time to breakdown versus electric field

CONCLUSION

An engraving storage electrode technology has been developed for enhancing the storage capacitance in DRAM, without reducing capacitor insulator thickness. A large capacitance of more than twice as that of the conventional technique was obtained by controlling the resist particle size of the engraving mask and the poly-Si etching-time. The resist particle size is controlled by (1) resist/SOG mixing ratio, and (2) thickness of the mixture coated on poly-Si storage electrodes.

A SiO_2/Si_3N_4 composite film exhibited excellent reliability even on the engraved storage electrode. This composite film meets both the leakage current and the time-to-breakdown requirements for DRAM applications.

Therefore, this technology is promising for 16 Mbit DRAM and beyond.

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REFERENCES

1] S. Kimura et al.; Ext. Abst. 19th Conf. on Solid State Devices and Mat. 19(1987)

2] T. Kisu et al.; Ext. Abst. 20th Conf. on Solid State Devices and Mat. 584(1988)

3] H. Shinriki et al.; Symp. VLSI Tech. Dig., 25(1989)

4] J. Yugami et al.; Ext. Abst. 20th Conf. on Solid State Devices and Mat. 173(1988)