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1 V·1 GHz Operating CMOS 1/8 Static Divider

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A CMOS divide-by-eight static frequency divider operating at 1.0 GHz and dissipating only 1.7 mW at a supply voltage of 1.0 V has been described. The corresponding power and power-delay products for the first stage toggle-type flip-flop (T-F/F) are 0.32 mW and 0.32 pJ, which are the best yet reported for any CMOS F/F. The divider owes its high performance to 0.2- μ m gate CMOS process technology and a new differential static T-F/F circuit. This new static T-F/F can be applied to the dual-modulus prescalar IC, which is a key component in the frequency synthesizer for personal telephone systems.

Introduction

CMOS circuits continue to make impressive strides forward in speed-power performance by shrinking device dimensions. Recently, multigigahertz CMOS IC's such as frequency dividers and prescalars using deep submicrometer gate-length CMOS technology have been reported [1][2]. These circuits with very low power dissipation will be key components in future battery-operated personal communication equipments.

At the same time, power supply voltage scaling has become increasingly important for avoiding reliability problems, which are caused by hot-carrier injection and oxide breakdown. Values of less than 2.0 V are considered necessary for sub-0.25 μ m gate NMOS [3][4].

In sum, to obtain both GHz-operation with very low power consumption and good device reliability, new circuit design concepts for small supply voltages as well as novel downscaled MOS device structures are demanded. In this paper, a CMOS 1/8 frequency divider operating at 1.0 GHz at a supply voltage of only 1.0 V is described. The divider owes its high performance to deep submicrometer gate CMOS process technology and a new T-F/F circuit.

0.2- μ m gate CMOS process technology

The CMOS devices were fabricated with a new isolated p-well structure for deep sub- μ m BiCMOS LSI [5] and designed with the 0.6- μ m rule except for the 0.2- μ m gate lengths. A single phosphorous-doped poly-Si gate, a 3.5-nm-thick gate oxide, and a single drain structure with an 0.08- μ m junction depth were used. The CMOS device parameters and measured I/V characteristics are listed in Table 1. This process yields inverter chain delay times of 34 and 96 ps at supply voltages of 2.0 and 1.0 V, respectively.

Table 1 0.2- μ m gate CMOS device

	PMOS	NMOS
Gate oxide thickness	3.5nm	
Junction depth	0.08μm	
Gate length	0.24μm	0.18μm
Gate width	12.0μm	7.5μm
Threshold voltage	-0.30V	0.25V
Transconductance at Vdd=2V	283mS/mm	312mS/mm
Subthreshold swing	101mV/dec.	78mV/dec.
Inverter chain delay time	34ps at Vdd=2V 96ps at Vdd=1V	

New Circuit Configuration

Fig. 1 shows the block diagram of the 1/8 frequency divider IC, which contains three T-F/F's connected in series, a clock buffer, an internal buffer, and an output buffer. A new differential static T-F/F, shown in Fig. 2(a), was used in place of the conventional dynamic and static T-F/F's shown in Figs. 2(b) and (c), respectively. The new T-F/F consists of two transfer-gate (TG)-type dynamic D-F/F's (Fig. 2(b)), whose inverters are cross-coupled through clock-input TG's. These cross-coupled inverter circuits hold their states statically.

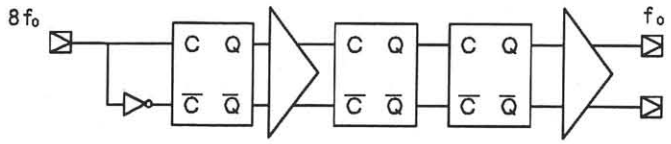

Fig.1 Block diagram of 1/8 frequency divider

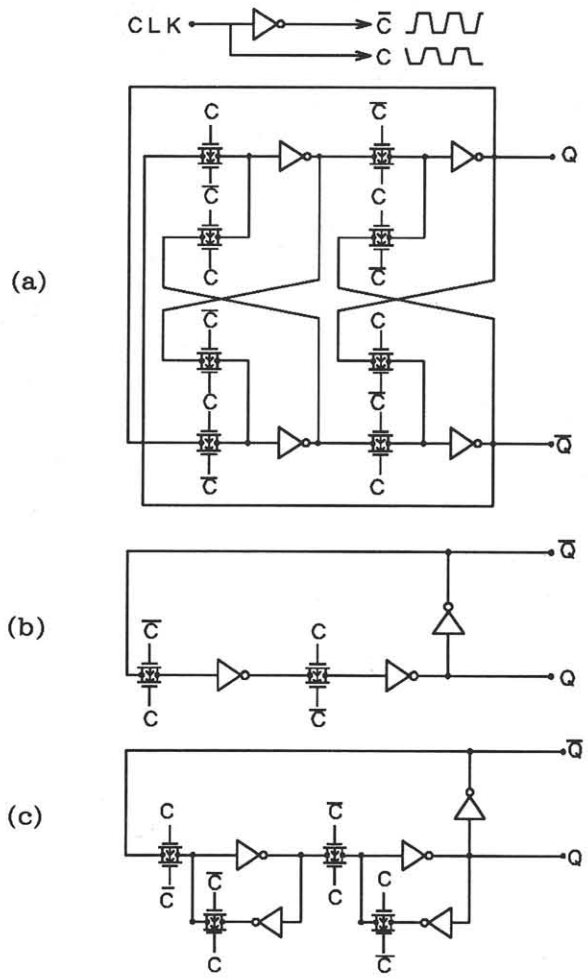

Fig.2 Circuit schematics for (a) new differential T-F/F, (b) conventional TG-type dynamic T-F/F, and (c) conventional static T-F/F.

In this differential configuration, the number of stages in the critical path is reduced by eliminating the inverter which generates the complementary output in the conventional T-F/F's [Fig. 2 (a) and (c)]. This concept can be also applied to the clocked-inverter (CI)-type dynamic D-F/F [1]. In this case, the CI-type differential T-F/F holds its state using cross-coupled CI circuits.

Circuit Performance

The measured maximum operating frequency and associated power dissipation as a function of supply voltage for the dividers composed variously of the new and conventional T-F/F's are compared in Fig. 3.

It is noteworthy that the speed performace for the new static divider is superior to that for the dynamic divider at a supply voltage below 1.5 V. In addition, the new T-F/F was found to offer wider operation margin at small supply voltages against deviation from designed device parameters such as threshold voltages.

The new divider is still functional at 1 GHz with the supply voltage as low as 1.0 V, dissipating only 1.7 mW of power.The corresponding power and power-delay products for the first stage T-F/F are 0.32 mW and 0.32 pJ, which are the best yet reported for any CMOS F/F. The operating waveforms at an input frequency of 1.0 GHz are shown in Fig. 4.

The minimum voltage swing (Vp-p) of the input sine wave signal needed by the divider as a function of input frequency for the range 10 MHz to 1.5 GHz is shown in Fig. 5. An input voltage sensitivity of less than 700 mVp-p was confirmed for operation from 30

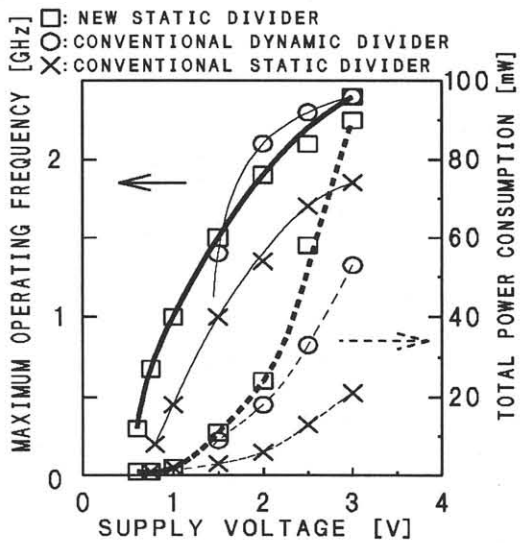

Fig.3 Maximum operating frequency and associated power dissipation versus supply voltage for the new static and the conventional 1/8 dividers. Power consumed in the output buffer driving a 2.7-pF external load is included in this data.

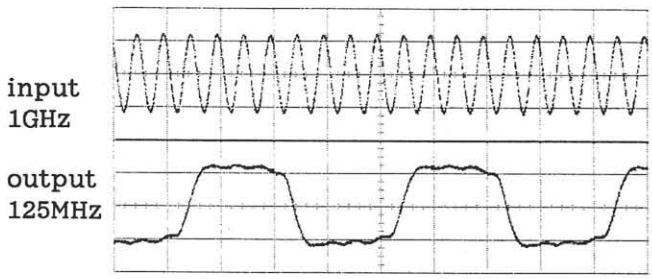

Fig.4 Operating waveforms of the input and output signals for the new static 1/8 divider operating at 1GHz. The power dissipation was 1.7mW (including output buffer) at Vdd=1.0 V. 400mV/div. ; 2ns/div.

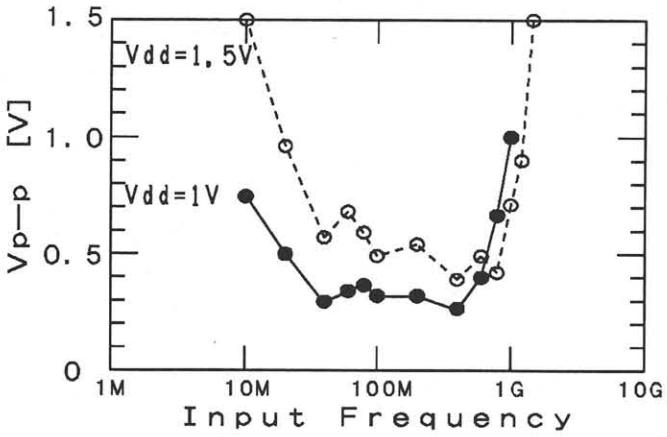

Fig.5 Minimum voltage swing (Vp-p) of input sine wave signal required for operation as a function of frequency.

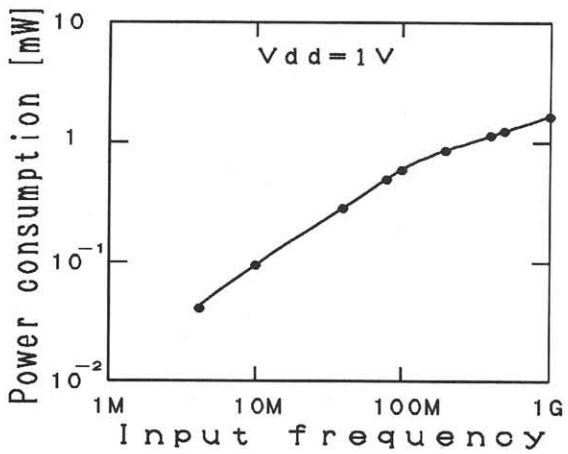

Fig.6 Total power consumption (including power consumed in the output buffer with 2.7 pF external load) as a function of operating frequency.

MHz to 1 GHz at a supply voltage of 1.5 V. Of course, the static divider is functional in the input frequency range from DC to 10 MHz when the input is driven by a step waveform.

The total power dissipation for the 1/8 dvider versus toggle-frequency is shown in Fig. 6. The power consumption is proportional to frequency up to 100 MHz. Above that the power saturates. This may indicate that the internal voltage swing decreases at high input frequencies.

This new static T-F/F can be used in the dual-modulus prescalar IC, which is a key component in the frequency synthesizer for personal telephone systems. In order to verify the performance of the new T-F/F in such applications, a ÷ 128/129 dual-modulus prescalar was simulated with SPICE, using the measured characteristics of the T-F/F. The simulated prescalar IC operated as fast as 1 GHz at a supply voltage of 1.2 V, dissipating only 2.4 mW. This power consumption can be reduced to less than 1.1 mW by fully scaling

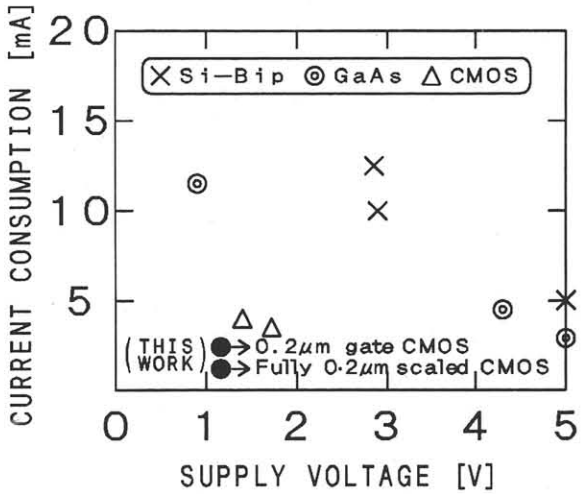

Fig.7 A comparison of simulated performance to other state-of-art divide-by-128/129 dual modulus prescalars operating at 1 GHz. Device technologies are also shown. The simulated results include power consumed in the output buffer with a 1-pF external load.

the devices down to 0.2 μ m. A comparison of these simulated results to the published results of other state-of-the-art prescalars is made in Fig. 7. It indicates the potential of the technologies demonstrated here to achieve multigigahertz integrated circuits with very low power consumption.

Conclusion

A 0.2- μ m gate CMOS 1/8 static divider has been designed and fabricated. The design of the T-F/F is accomplished using a new " differential configuration " concept. The circuit operates up to 1.5 GHz at supply voltage of 1.5 V. A supply voltage of only 1 V is sufficient for 1 GHz operation, dissipating only 1.7 mW with a 2.7 pF external load. These results indicate that the high speed and very low power features of this divider should have an important impact on the development of future personal communication systems.

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