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Advanced Ti Salicide Technology for High Performance Quarter-Micron Logic LSIs

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An advanced Ti salicide technology is proposed for high performance quarter-micron logic LSIs. A new salicide process named ESPAD (Enhanced Silicidation with Pre-Amorphization using Direct ion implantation) in combination with an optimum RTP (Rapid Thermal Processing) and furnace annealing has been developed. The formed $TiSi_2$ is able to maintain low sheet resistance even in narrow (0.2 μ m) S/D region to achieve minimum basic cell size and low junction leakage current. High performance logic LSIs with low stand-by current are fabricated using this technology.

1. Introduction

Ti salicide technology is widely used to reduce the parasitic resistance for high performance logic LSIs. In conventional $TiSi_2$ technology, the sheet resistance increases in narrow regions in the C49-$TiSi_2$ crystal phase. In order to improve such sheet resistance characteristics, a pre-amorphized Ti salicide process with additional annealing was developed to form stable C54-$TiSi_2$ crystal phase [1]. However, $TiSi_2$ over-growth is resulted on the LDD sidewall spacer and field oxide area by such additional annealing. On the other hand, Co salicide technology has been also proposed as a substitute for $TiSi_2$ in smaller than quarter-micron devices because of its stable low sheet resistance in narrow regions [2] [3]. In this paper, we propose a new process named ESPAD (Enhanced Silicidation with Pre-Amorphization using Direct ion implantation) useful for quarter-micron logic LSIs as well as Co salicide.

2. Process Flow

2.1 Source/Drain Process Module

A process flow for CMOS fabrication is shown in Fig. 1. For the formation of Nch S/D region, As ions were directly implanted into the Si substrate in order to prevent the Si substrate from being contaminated by knocked-on oxygen from the oxide. After the Nch S/D implantation, furnace annealing was used in O_2 ambient for the stress relaxation at the LDD sidewall and LOCOS edges. BF_2 ions were implanted into the Si substrate through SiO_2, where the fluorine obstructs the silicide reaction being trapped in this SiO_2 layer and the boron passes through to the Si substrate. Next, activation RTA was used at 1000 ℃ for 10 sec with controlled heating and cooling rates of 10 ℃/sec. After the activation annealing, furnace annealing was applied at 800 ℃, where residual Si crystal defects recover completely and the junction depth does not increase. Moreover, at the gate sidewall edges and LOCOS edges, stress was relaxed by these heat treatments [4]. As a result, no Si crystal defect was generated after the silicide formation on the S/D region.

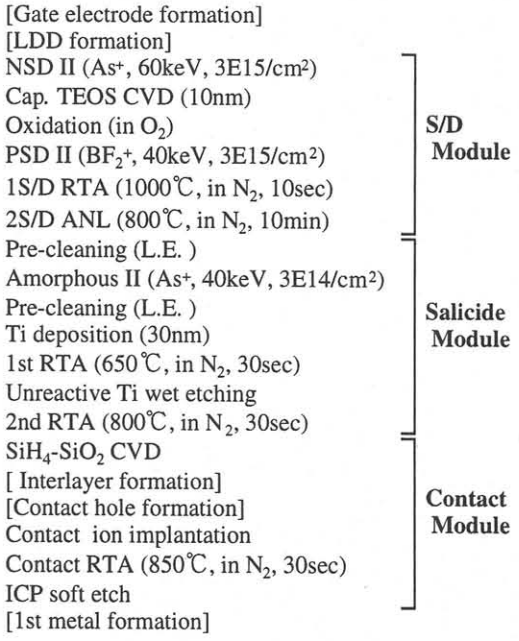

Fig. 1. Process flow for CMOS fabrication.

2.2 Ti Salicide Process Module

After complete cleaning on the Si surface using an HF solution, As ions were implanted into the Si surface to amorphize. When the residual oxide exists on the surface of the Si substrate without that cleaning, the oxygen, which is implanted from the oxide by collision with As ions at the surface, obstructs the C-54 $TiSi_2$ phase formation by silicidation annealing. After the Ti deposition, salicide was formed at the S/D regions by 2 step annealing method.

2.3 Contact Process Module

CVD SiH_4-SiO_2 and CVD O_3-TEOS-SiO_2 as an interlayer were deposited on the $TiSi_2$. When the CVD O_3-TEOS-SiO_2 was directly deposited on the $TiSi_2$, a contact resistance was unstable after contact formation because of oxidation of $TiSi_2$ by active O_3.

For fabrication of logic LSIs with minimum cell area, it is necessary to use contact ion implantation process in order to suppress contact leakage current caused by etching at

LOCOS edges when contact alignment error occurs. After contact hole formation in cells of logic LSIs, contact ion implantation and activation RTA were used at 850 ℃ for 30 sec with controlled heating and cooling rates of 10 ℃ /sec. Agglomeration and oxidation of $TiSi_2$ surface are suppressed in this condition. Before metallization, ICP (Inductively Coupled Plasma) soft etching with Ar ions was used as in-situ premetallization [5].

3. Results and Discussion

Fig. 2 shows the cross-sectional SEM micrograph of a developed logic LSI. Uniform $TiSi_2$ can be formed even in narrow regions. Furthermore, over-growth of the silicide on the sidewall and field oxide regions is completely prevented by the ESPAD process. Fig. 3 shows plane view TEM micrograph of ESPAD $TiSi_2$ on 0.2 μ m width N^+ diffusion region. In the ESPAD process, stable C-54 phase $TiSi_2$ can be formed even in such narrow region.

Dependence of sheet resistance on diffusion layer line width is shown in Fig. 4. Low sheet resistance at less than 0.25 μ m can be obtained using the ESPAD-$TiSi_2$. On the other hand, the sheet resistance of $TiSi_2$ formed by conventional 2step annealing process begins increasing at 1.0 μ m width.

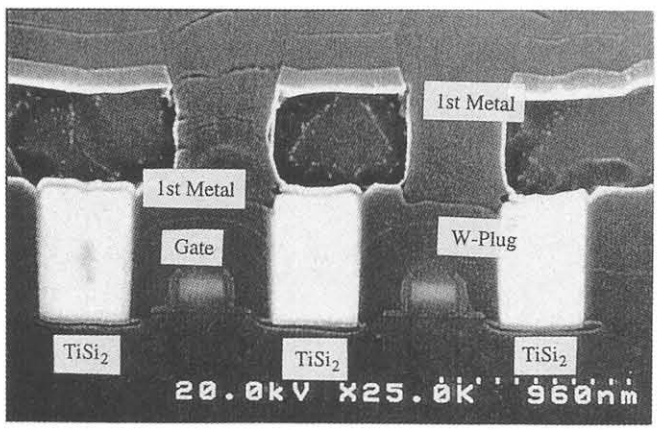

Fig. 2. Cross-sectional SEM micrograph of a developed logic LSI.

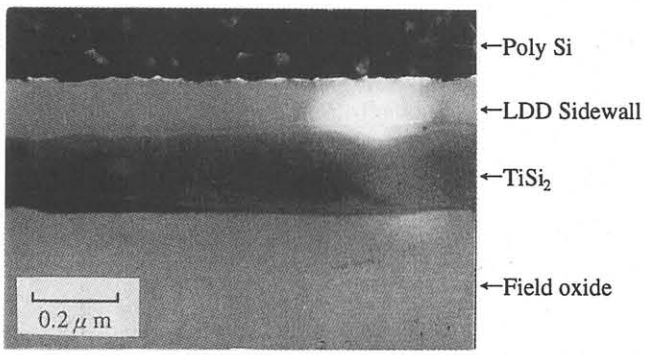

Fig. 3. Plane view TEM micrograph of ESPAD $TiSi_2$ on a 0.2 μ m width N^+ diffusion region.

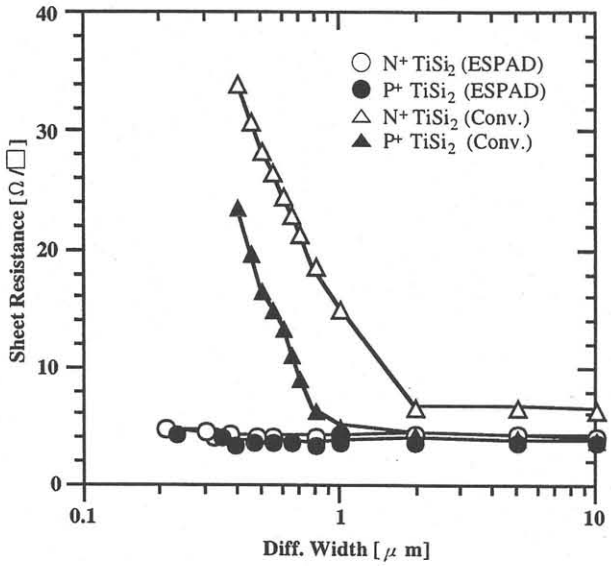

Fig. 4. Sheet resistance of a $TiSi_2$ as a function of diffusion layer width.

Junction leakage current characteristics are shown in Fig. 5. Using the optimized annealing processes (oxidation after NSD II, 2S/D ANL, and RTA processes with controlled heating and cooling rates of 10 ℃/sec), stable $TiSi_2$ can be formed on the S/D region and low junction leakage levels are maintained.

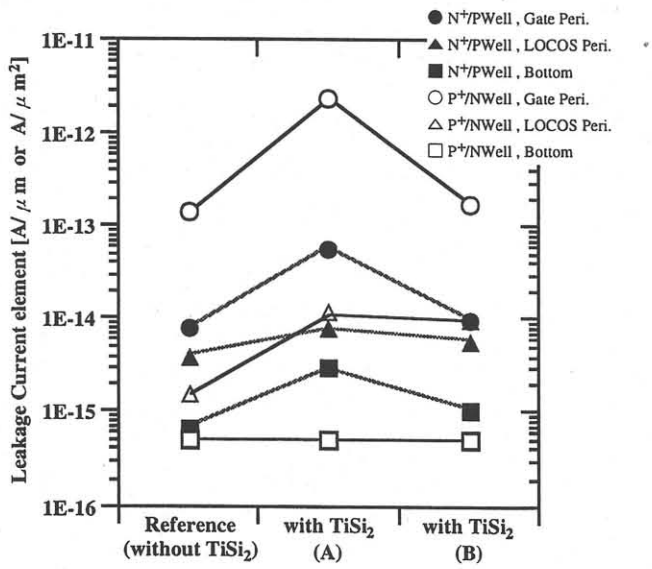

Fig. 5. Junction leakage current characteristics.
(A) Without optimum annealing process.
(B) With optimum annealing process.

Fig. 6 shows a cross-sectional TEM micrograph at the bottom of the contact hole on N^+ $TiSi_2$ using furnace annealing for contact activation. $TiSi_2$ surface is oxidized by the atmosphere. The oxide can not be etched off easily by the ICP soft etching with Ar ions and obstructs ohmic contact formations on $TiSi_2$. We observed the oxidation by EDX (Fig. 7). On the other hand, using RTA for the

annealing, it is possible to suppress the oxidation and to form stable ohmic contact. Removing the oxide from salicide processes is one of the most important matters.

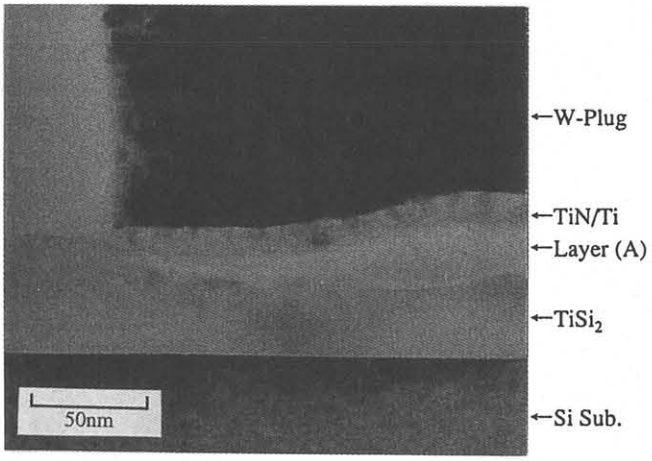

Fig. 6. Corss-sectional TEM micrograph at the bottom of contact hole on $TiSi_2$, using furnace annealing for contact activation.

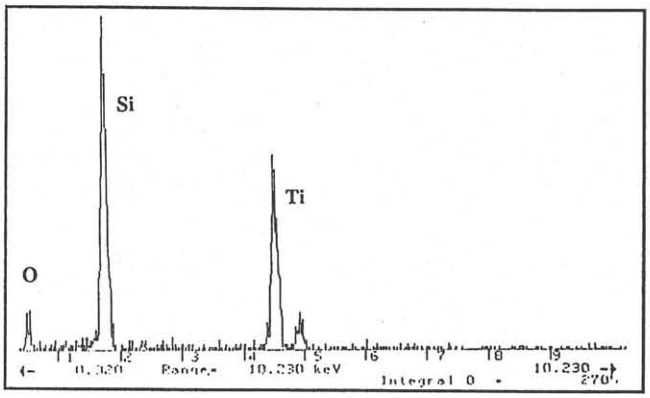

Fig. 7. EDX spectra at the layer (A) indicated in Fig. 6.

A CMOS transistor with the ESPAD-$TiSi_2$ has superior drivability. We also estimated the CMOS performance with a bending gate structure with S/D width of 0.2 μm (Fig. 8). As the ESPAD-$TiSi_2$ is able to maintain low sheet resistance even in regions of smaller than 0.2 μm in the width, excellent V_d-I_d characteristics of CMOS with ESPAD-$TiSi_2$ are obtained (Fig. 9).

4. Conclusion

We have demonstrated that the ESPAD-$TiSi_2$ with an advanced CMOS module process is highly effective for obtaining low sheet resistance. It is also necessary to optimize annealing processes and contact formation processes for obtaining low leakage current and stable ohmic contact in such Ti salicide devices. This technology is particularly effective for the development of quarter-micron logic LSIs.

5. Acknowledgment

The authors would like to thank H. Masuya for her TEM analysis and staffs at Process Line Department for help in the device fabrication.

6. References

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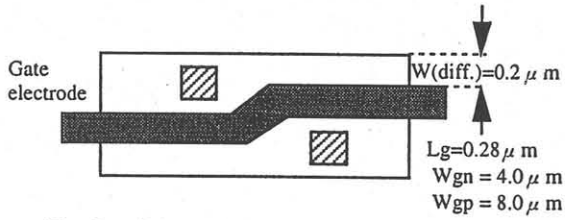

Fig. 8. Schematic diagram of bending gate Tr.

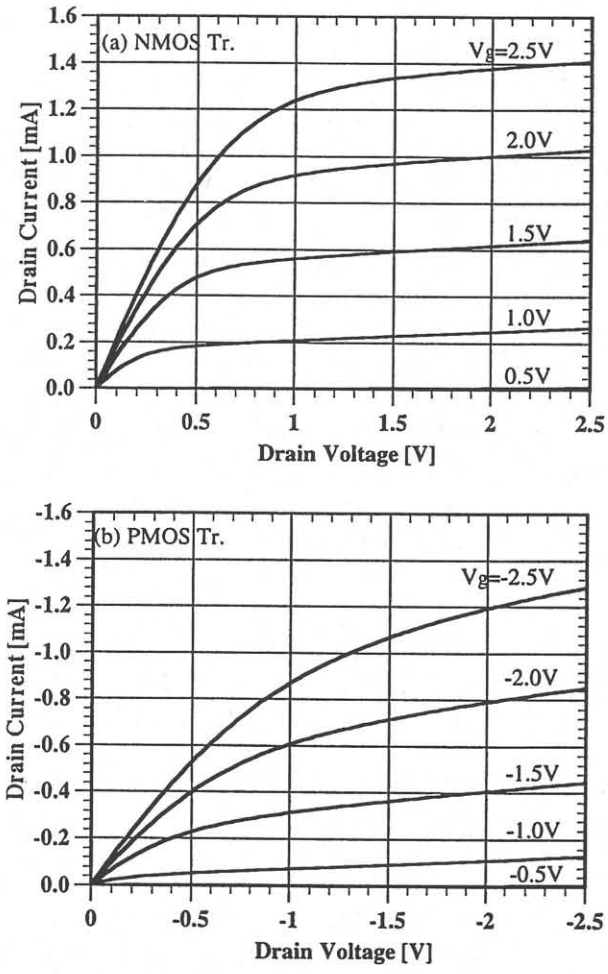

Fig. 9. V_d-I_d characteristics of (a) NMOS bending gate Tr. and (b) PMOS bending gate Tr. with ESPAD-$TiSi_2$