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Excess Noise in Sub-Micron Silicon FET:Transport Theory and Device Optimization

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1. Introduction

Deep sub-micron CMOS FETs develop *excess noise* due to the *"heating"* of carriers by the high lateral electric field in the channel. This work reports theoretical and experimental results that relate the *"excess noise"* produced in these FETs to the effective masses of the carriers, transport modes, and the carrier concentration profile along the device channel, thus providing guidelines for device optimization for low noise operation.

The *Ergodic Method* [1], [2] relates the current noise in a non-degenerate slice of semiconductor material to the *variance* in carrier velocity distribution. According to this approach to noise phenomena, low noise operation under **high electric fields** is achieved via forcing the carriers to travel with the narrowest possible distribution[1].

Recalling the Boltzmann Transport Equation:[3]

$$\frac{\partial f}{\partial t} + \boldsymbol{v}.\boldsymbol{\nabla}_{\boldsymbol{r}} f + \frac{q}{m^*}\boldsymbol{E}.\boldsymbol{\nabla}_{\boldsymbol{p}} f = \left.\frac{\partial f}{\partial t}\right|_{coll} \qquad (1)$$

The effective mass of the carriers modulates the *carrier heating* effect produced by the applied electric field; and the carrier concentration profile can be used to make the term $\boldsymbol{v}.\boldsymbol{\nabla}_{\boldsymbol{r}} f$ counter balance the *heating effect* produced by the field via $\frac{q}{m^*}\boldsymbol{E}.\boldsymbol{\nabla}_{\boldsymbol{p}} f$.

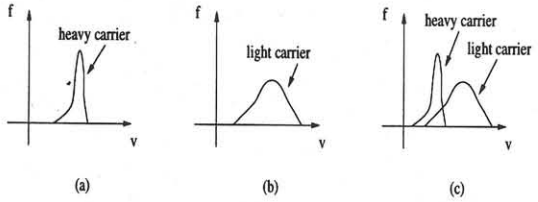

Fig. 1. Conceptual velocity distributions of carriers in high electric field transport. (a) heavy-effective-mass, lower variance, (b) light-effective-mass, higher variance (c) heavy and light effective-mass, higher **total** variance.

Thus in **high electric field** transport: 1) A heavier carrier based device develops less excess noise than a light carrier based device; 2) Low noise devices need to have carriers traveling with *only one effective mass* (*"single mode transport"*); and 3) Graded doping profile can be used to minimize excess noise generation.

2. Experimental Developments

The experimental setup for low noise measurements is depicted in figure 2.

Testing the setup with known values of resistance, the noise levels measured for *low electric field transport* follow the thermal noise expression, $\overline{i^2} = 4GK_BT_L\Delta f$. These low field noise measurements fall along the straight line

[1]In this approach, the *thermal noise* equation (Nyquist Theorem) is recovered as an special case when the DC current or the applied electric field goes to zero.

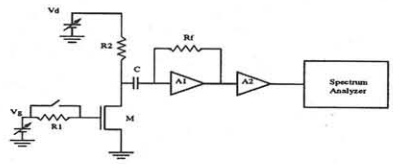

Fig. 2. Description of the system designed for measurement of drain current noise power of FETs.

shown in fig. 3. Sub-micron transistors under **high electric field transport** develop *"excess noise"* in the channel, and fig. 3 shows typical experimental results, which diverge from the straight line of low noise measurements as V_{DS} is increased. (The gate noise contribution was negligible)

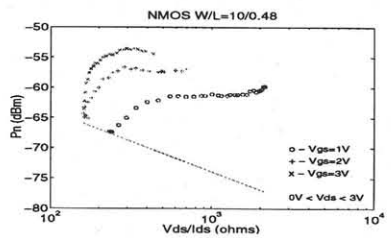

Fig. 3. High field current noise power of NMOS transistor. $W = 10\mu m$ and $L_{eff} = 0.48\mu m$.

The *excess noise factor*, γ_f, is *defined in this work* as the separation between the excess noise level developed by the transistor at each bias point and the thermal noise developed by a *hypothetical thermal resistor* with resistance value equal to V_{DS}/I_{DS} (fig. 4). Note this γ_f is **different** from other author's.[4], [5]

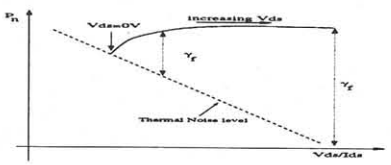

Fig. 4. γ_f and high field *excess noise* in FETs. Dashed line is *thermal noise level.*

The drain current noise is expressed as $< i^2 > /\Delta f = 4GK_BT_L\gamma_f$. A typical plot of γ_f *vs.* the *average lateral electric field in the channel*, V_{DS}/L_{eff}, is shown in fig. 5. The FET with curve 5(a) has a γ_f diverging from *"1"* (thermal noise level) faster then the FET 5(b). Therefore FET 5(b) is the less noisy device.

Effective Mass and Noise:

Fig.6 shows experimental results for γ_f of NMOS and PMOS devices with dimensions of W/L_{eff}: 40/0.4,

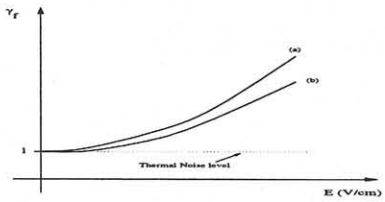

Fig. 5. γ_f, function of electric field. $\gamma_f = 1$ for no field, i.e. $V_{DS} = 0V$. (a) is an FET noisier than the FET described by (b).

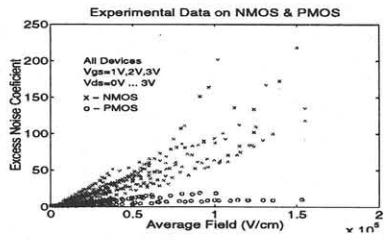

Fig. 6. γ_f for Si NMOS ("x") and PMOS ("o").

10/1.38, 10/0.78, 10/0.48, 10/0.23, 10/0.18; W and L_{eff} in microns.

Electrons are much lighter than holes in Si, and accordingly NMOS develops more *excess noise* in high fields than PMOS for **all** device sizes tested. The spreading on γ_f for NMOS and PMOS is due to the carrier concentration profile for different device lengths.

Transport Modes and Noise:

Figure 7(a) depicts the Si-on-SiGe FET structure [2] used for these experiments.

In bulk Si, if the the DC electric current flows in the $< 010 >$ direction, electrons will travel with either *transverse effective mass* or *longitudinal effective mass*(fig. 7(b)). Biaxial stress offsets the horizontal constant-energy ellipsoids from the vertical ellipsoids. Strained Si with current in $< 010 >$ will have electrons *"only"* in the vertical ellipsoid, thus having *"only" transverse effective mass* transport mode (fig. 7(c)).

Plots of γ_f for Si-on-SiGe FETs 10% Ge and 30% Ge are depicted in fig. 8. The more *"single mode"* 30% Ge FETs develop less excess noise than the 10% Ge FETs. *"Self heating"* effects on Si-on-SiGe FETs preclude them from being the lowest noise performer at high current levels.

Carrier Concentration Profile and Noise:

There are many carriers at the *source* and the carrier distribution is Maxwellian there. Inside the channel, there are fewer carriers available, and the distribution shifts and is centered at a higher value of velocity. This shift

[2] J. Welser et al., IEEE IEDM 1994, p. 373.

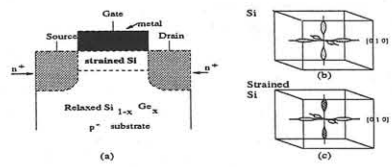

Fig. 7. Si-on-SiGe FET (a), bulk Si (b), and Strained Si (c). More Ge in The $Si_{1-x}Ge_x$ layer leads to more strain in Si, and more "single mode" transport.

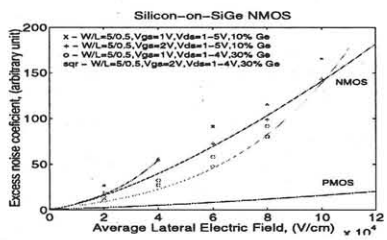

Fig. 8. The 30% Ge Si-on-SiGe FETs ("o", squares) develops much lower levels of excess noise than the 10% Ge ("x","+"). Same length NMOS and PMOS curves are plot for comparison. Eye-aid curves added.

is felt as a *"push"* that augments the *variance* in carrier velocity distribution. The *graded channel MOSFET* (fig. 9) softens this *"push"* by providing **more** carriers for transport, as carriers progress from *source* to *drain.*

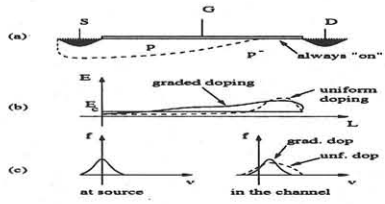

Fig. 9. Graded channel n-MOSFET. (a) structure, (b) electric field better distributed than uniform doped FET, and (c) less variance in velocity distribution, hence less noise in **high electric fields**.

Fig. 10 shows γ_f for the graded channel MOSFET and uniform sub-micron NMOS and PMOS FETs of the same gate length. Note that the graded channel MOSFET is a n-MOS device, and that it performs very close to standard sub-micron PMOS transistors, which use much heavier carriers (*holes*).

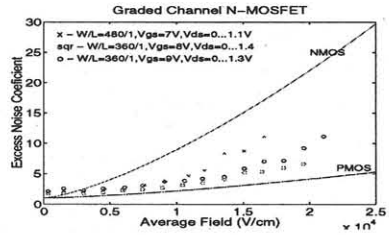

Fig. 10. Excess noise factor for graded channel n-MOSFET ("x","o", and squares). Uniform NMOS and PMOS curves also plotted for comparison.

3. Conclusion

Excess noise of sub-micron CMOS FETs is controllable. Low noise device design should force the carriers to travel with the narrowest possible distribution, by either tailoring the carrier effective masses or doping profiles.

References

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[2] L.M. Franca-Neto, and J.S. Harris, IEEE Top. Mtg. on SiMIC in RF Sys., Sep. 1998.
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