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A Novel High Responsivity, Wide Band Silicon Photodiode

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1. Introduction

Recently, silicon photodiode has been the focus of attention as a widely used standard detector for CCD imager, pattern recognition and front-end receiver for the modern OEIC (Opto-Electronic Integrated Circuit) [1-2]. This is due to its simple layout and ease to fabricate together with other circuitries on the same chip at a lower cost [3]. However, little study on the effects of silicon photodiode layouts design and optimization on the IV characteristics as well as high frequency behaviors have been reported. An extensive study of various layout design of silicon photodiode is presented in this paper. High frequency behaviors, IV and CV characteristics of photodiodes, fabricated using the standard 0.25μm CMOS technology is reported.

2. Photodiode Design and Fabrication

A P Type, <100> silicon wafer with a resistivity ρ = 7.5 Ω-cm was used for the fabrication. Using the N-well mask, well implantation was carried out with a doubly-charge Phosphorus at an energy of 490keV and a dose of $2\times10^{13}cm^{-2}$. The N-well depth is about 1.4μm from the surface. Arsenic (60keV, $3\times10^{15}cm^{-2}$) implant and BF_2^+ (40keV, $3\times10^{15}cm^{-2}$) implant were used to form the N^+ and P^+ regions, respectively. The N^+ and P^+ diffusion depths were found to be around 0.25μm with a sheet rho of 100Ω/sq. Finally, aluminium self-aligned-silicide (salicide) process was performed to reduce the contact resistance of the N^+ and P^+ regions.

The top view of the layout and the cross sectional view of the fabricated photodiodes is illustrated in Fig. 1. The diameter of all the photodiodes is fixed at 75μm. The outside circular guard ring is the P^+ region of the diode. Its width and the distance from N^+ region are fixed at 1μm, and 1.6μm, for all the layout styles. For **PD1**, in Fig. 1(a), the inside circular part is the N^+ cathode region of the diode. The ohmic contact is made only at the corner of the N^+ region to receive the maximum exposure of light. In this layout, the PN junction is formed mainly between the bottom part of the N^+ region and the P-substrate. To maximize the depletion region of sidewall and bottom area, N^+ region in **PD2** is designed as concentric circle with multiple circular N^+ regions, as shown in Fig. 1(b). The distance between each N^+ region is kept at 0.6μm. For **PD3,** an N-well is placed between the P^+ and N^+ diffusion region as shown in Fig. 1(c). In this layout, P^+ and N^+ regions become the contact for P-substrate and N-well, respectively. As a result, a depletion region is formed between the N-well and P-substrate.

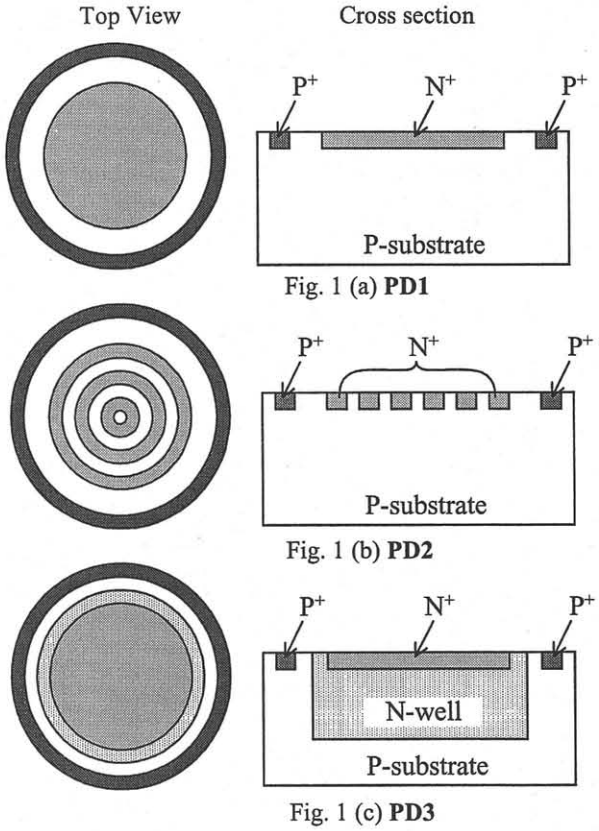

Fig. 1 (a) **PD1**

Fig. 1 (b) **PD2**

Fig. 1 (c) **PD3**

Fig. 1 Layout top and cross sectional view of fabricated photodiodes.

3. Results and Discussion

The dependency of photocurrent on the illuminated light intensity is illustrated in Fig. 2 for a reverse bias of 1V. The photocurrent increases linearly with the light intensity for all photodiodes. It can be clearly seen that N-well photodiode is more sensitive than the N^+ junction

photodiodes regardless of illumination intensity. This is due to two main reasons: (a) N-well junction is composed of two parts, sidewall (deeper than N^+ region and hence larger depletion region) and bottom area, (b) N-well depletion region is much wider because its doping concentration is about two orders lower than the N^+ region. However, its advantage over the N^+ photodiode can be lost for shorter light wavelength because most of the photons are absorbed before reaching to the depletion region. For the given area and with a light intensity of $20mW/cm^2$, the N-well photodiode produces a photocurrent of around 12μA while maintaining a dark current of $0.16nA/cm^2$.

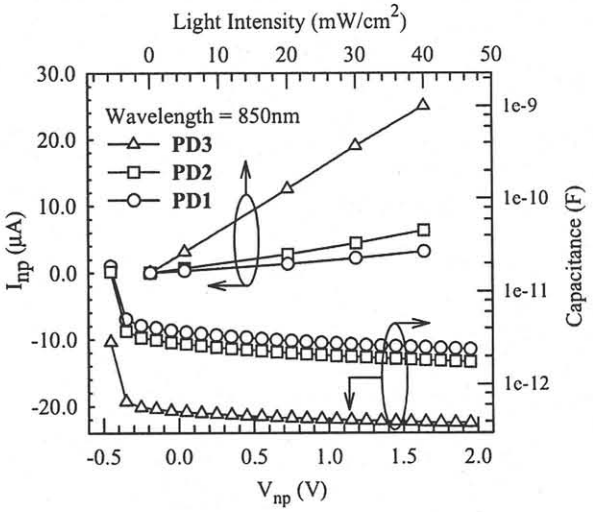

Fig. 2 CV characteristics and photocurrent versus light intensity of the fabricated photodiodes.

Photodiode capacitance is the primary limitation for the circuit design because it significantly affects the signal bandwidth and the rise and fall time of the photodiode. In Fig. 2, the measured diode capacitance is plotted against the reversed bias voltage. The measured capacitance is composed of sidewall and bottom junction capacitance and was measured at a frequency of 1MHz and an oscillation voltage level of 150mV. Form Fig. 2, **PD3** gives the lowest capacitance while **PD1** has the highest capacitance value. A little improvement in total capacitance is observed for **PD2** when compared to that of **PD1**. Because the bottom junction capacitance contributes to a larger portion of the total capacitance for the PN junction, this improvement in total capacitance comes from the reduced bottom junction capacitance of the concentric layout, in which the bottom depletion region (i.e. **PD2**) is considered to be smaller than that of **PD1**. Substantial improvement in capacitance is observed for **PD3** as compared to **PD1** and **PD2** due to a lower doping concentration of the N-well and P-substrate. For the given photodiode area, the measured capacitance for **PD3** at a reverse bias voltage of 1V is 0.5pF.

High frequency response of photodiodes is illustrated in Fig. 3. Frequency responses are measure in frequency domain with a reversed biased of 1V and a light intensity of $30mW/cm^2$. As shown in Fig. 3, the 3dB bandwidth for **PD1**, **PD2** and **PD3** are found to be 384MHz, 493MHz and 6.27GHz, respectively. The frequency response of **PD3** at reversed bias voltage of 2.5V and 5V are also shown in Fig. 3. The photodiode bandwidth increases with the reversed biased due to decreasing photodiode capacitance. A bandwidth as large as 9.4GHz is achieved at a reversed bias of 5V. The highest bandwidth for silicon photodiode reported so far.

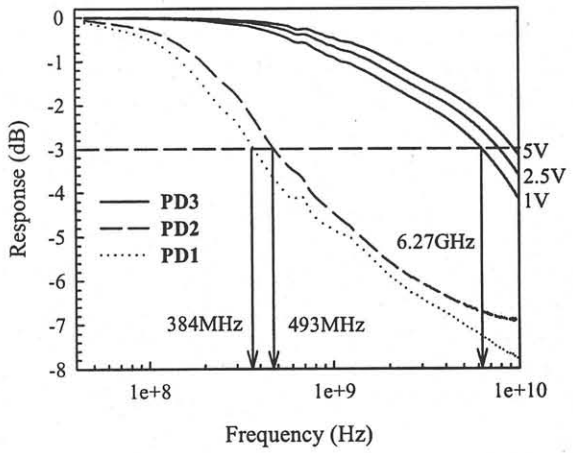

Fig. 3 High frequency response of fabricated photodiodes.

4. Conclusions

The layout design and optimization of high performance silicon photodiodes fabricated using a 0.25μm CMOS technology is reported. Photodiode IV characteristic, dark current, diode capacitance, and high frequency response of various layout design are compared under a wide range of light intensity, frequency and reversed bias voltage. It is found that the concentric circle layout outperforms other conventional N^+-P junction. A high performance N-well photodiode with a bandwidth as large as 9.4GHz at 5V and a capacitance as low as 0.5pF is also demonstrated.

References

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