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Organic Transistors for Logic and Flexible Display Applications

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I. Introduction

Organic circuits are of interest for applications where low cost, large area, or flexibility are required, such as displays, electronic shelf-tags, and wireless identification tags (1-4). Realization of the promise of organic electronics for low-cost, large area, circuits relies on the development of fabrication methods which are very different from conventional lithography and more conducive for implementation in reel-to-reel production formats, and on circuit designs which take advantage of the properties of organic semiconductors. Organic transistors have also been integrated with display elements such as light-emitting diodes (5,6).

II. Experimental Methods

Several low cost fabrication methods have been explored by our group: screen printing, microcontact printing, and soft lithographic techniques that can result in feature sizes as small as 0.1µm (7,8). Noble metals such as Au form good ohmic contacts with both hole transporting (for p-FETs) and electron transporting organic semiconductors. We have developed techniques for the electroless deposition of Ni and immersion coating of metals such as Au, Pt, and Pd for the source drain electrodes on a variety of sensitized surfaces. Electroless Ni/Au or Ni/Pd results in excellent electrical contacts as well as superior mechanical properties. Furthermore this approach can be combined with other patterning techniques used to define the areas of deposition.

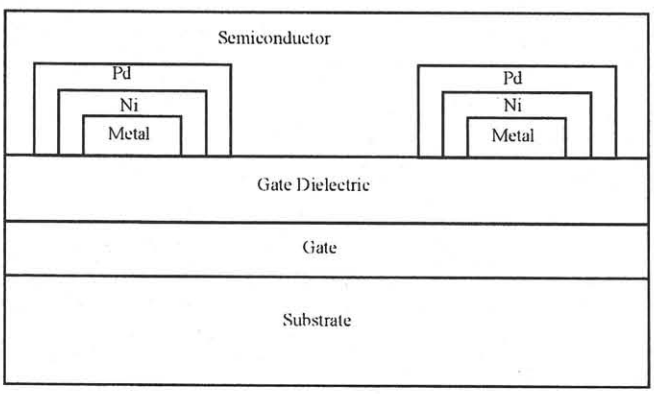

Figure 1 Schematic structure of an organic FET with source / drain regions formed by electroless deposition of Ni / Au on a metal surface.

Figure 1 illustrates the layer structure of a typical device. Organic semiconductors are deposited as the final layer on such substrates to form FETs. In this work hexadecaflourocopper phthalocyanine ($F_{16}CuPc$) is used for n-channel FETs, and α-sexithiophene (α6T) or dihexyl α-quinquethiophene (DHα5T) are used for p-channel FETs.

III. Results and Discussion

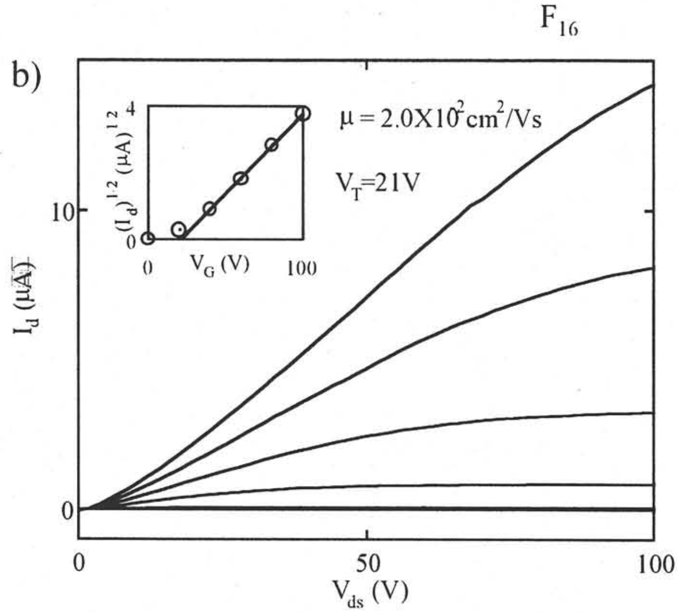

Figure 2 shows the DC characteristics of discrete an n-channel (FCuPc) with W=100µm and L=7.5µm. Drain current is plotted versus source drain voltage for gate voltages from 0 to 100 V. The inset of figure 2 shows $I_D^{1/2}$ versus V_g. These data are fit with a straight line to get the carrier mobility and threshold voltage.

Figure 3 shows the measured (solid line) and SPICE simulated (dashed line) characteristics of a 5-stage ring oscillator with FCuPc n and DHα5T p-channel FETs with W=2mm and L=7.5µm. SPICE simulation of DC characteristics of FCuPc n and DHα5T p-channel FETs gave $\mu = 5.2\times10^{-3}$ cm²/Vs and V_T=-1.2V for FCuPc, and $\mu = 1.6\times10^{-2}$ cm²/Vs and V_T=27.4V for DHα5T. The SPICE simulation used these parameters, except for the p-channel FET whose threshold voltage was taken as 10.4V to give better agreement for low voltage swings. The measured and simulated characteristics agree well, and show an oscillation frequency of 10kHz, for a propagation delay of 10μs per stage switch. This is larger than the gate switching time seen in the transient measurements (figure 3) because of the larger output impedance of the driving stage.

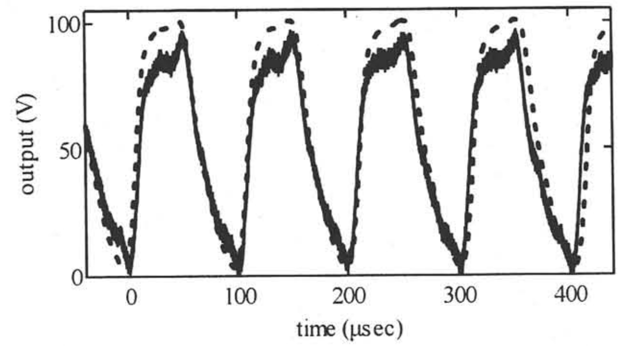

Figure 3 Measured (solid line) and simulated (dashed line) characteristics of a five stage complementary ring oscillator with FCuPc n and DHα5T p-channel FETs. All transistors have L=7.5μm and W=2mm.

We have fabricated shift registers based on two different D-flip-flop designs. The first is a logic gate based design which requires 48 FETs per flip-flop excluding output buffers. The second is a pass transistor logic based design with 16 FETs per flip-flop excluding output buffers. The logic gate based design should be more robust to large leakage currents, but will suffer more from propagation delay. The largest circuit demonstrated so far is a 48-stage shift register with 864 transistors (9).

The characteristics of complementary inverters fabricated on flexible plastic substrates employing micro-contact printing to pattern the sources and drains are shown in Figure 4. The gate dielectric employed in this circuit is a solution-cast polyimide. The channel length of the devices is 2 μm, and the fabrication process is described in detail in Ref.7.

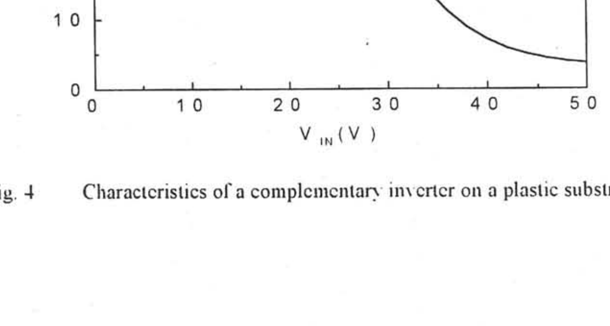

Fig. 4 Characteristics of a complementary inverter on a plastic substrate.

This demonstration suggests that the complementary circuits described above which have been realized on rigid substrates can be implemented on plastic utilizing low-cost soft lithographic patterning techniques.

Conclusions

We have demonstrated complementary organic circuits ranging in complexity from inverters through shift registers, using electroless deposition of Ni/Au source and drain electrodes. A number of fabrication methods suitable for organic transistor based circuits on flexible plastic substrates have been developed.

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