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Ultrathin Zr Silicate Gate Dielectrics with Compositional Gradation

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1. Introduction

High-k gate dielectrics, such as Zr silicates, have gained considerable attention because of their thermal stability [1,2]. The electrical properties of silicate/Si interfaces are improved with an increase of Si concentration. However, the permittivity decreases when metal concentration is low. Therefore, we need to optimize both the composition and structure of the films to obtain advantages for the gate stack.

In the current study, a Zr silicate gate dielectric with compositional gradation in depth is proposed. The silicate is composed of a tri-layer structure, which has Si-rich layers both at the top and the bottom of the film. Thus, we can obtain advantages of the silicate material while keeping sufficient permittivity. This paper describes the promising electrical properties of the silicate, such as the equivalent oxide thickness (EOT) and the improved Vfb shift by post deposition annealing (PDA).

2. Fabrication of Zr silicate with compositional gradation

Zr silicate films were fabricated by *in situ* reoxidation of thin Zr layers deposited on oxidized Si(001) wafers (Fig. 1). As we previously reported, an interfacial silicate reaction during reoxidation can be controlled through the SiO_2 thickness formed on the Si substrate [3,4]. In this experiment, a 0.3-nm thick SiO_2 was used and reoxidation was performed at 550℃ under $1x10^{-4}$ Torr oxygen.

Figure 2 shows changes in the Si2p and Zr3d photoelectron spectra during fabrication. Obviously, the Zr atoms were fully oxidized and the silicate bonds were formed after the reoxidation. A cross-sectional TEM image revealed a tri-layer structure with a compositional gradation in depth (Fig. 3). SIMS and HR-RBS analyses also showed that the Zr element is localized at the center of the silicate film and that the Si concentration increases both at the top and the bottom of the film, as illustrated in Fig. 3. These results indicate that silicate films (not pure ZrO_2) were formed through reoxidation, when 0.3-nm-thick SiO_2 is used. In this case, a considerable amount of Si atoms were supplied from the interface, and a part of the emitted Si atoms segregate near the surface [5] to form a Si-rich layer, as shown in Fig. 4.

3. Electrical properties of ultrathin Zr silicate films

Figure 5 represents a cross-sectional TEM image of a 2.6-nm-thick Zr silicate film. The thickness of the silicates and the Zr concentration were designed by the number of the Zr atoms deposited on the oxide. The tri-layer structure was clearly formed even for the ultrathin silicate film. The peak Zr concentration around the center of the film was 19%, and the average concentration was 7%.

Annealing of the ultrathin silicate was performed under various conditions in nitrogen ambient. Figure 6 shows a typical C-V curve obtained from the silicate film annealed at 500℃ for 10 minutes. The EOT was down to 1.1 nm, and the leakage current was less than 0.11 A/cm^2.

Figure 7 shows the EOT vs Jg characteristics of the ultrathin silicates treated by various PDA conditions. Annealing over 500℃ was required to reduce the leakage current. However, the EOT of the silicate increased due to interfacial oxide growth. Judging from Fig. 7, annealing at 500℃ for 10 and 30 minutes seems to produce suitable conditions for high-performance and low-power devices, respectively. In addition, as reported for Al_2O_3 [6], PDA is crucial for reducing the fixed charge at high-k/Si interfaces. Figure 8 shows changes in the Vfb as a function of the annealing temperature and time. These results indicate that the interfacial properties can be improved by optimizing the PDA conditions.

4. Conclusions

Ultrathin Zr silicate films with a compositional gradation in depth were fabricated by *in situ* reoxidation. The silicate exhibited encouraging EOT vs Jg characteristics (EOT: 1.1 nm, Jg: 0.11A/cm^2), and the fixed charge was found to be reduced by PDA. These results indicate that the compositionally graded silicate structure can improve both the thermal stability against crystallization and the electrical properties at high-k/Si interfaces.

Acknowledgments

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References

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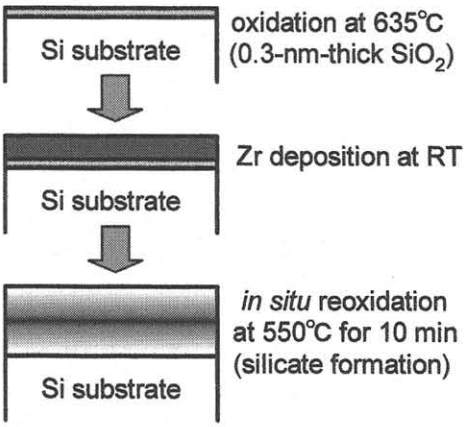

Fig. 1. Fabrication of Zr silicate films by *in situ* reoxidation.

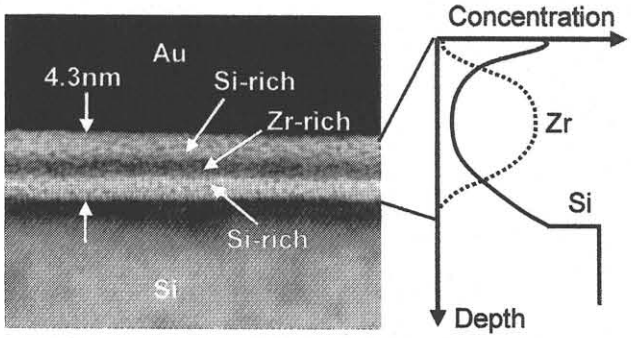

Fig. 3. Cross-sectional TEM image of a Zr silicate film with compositional gradation.

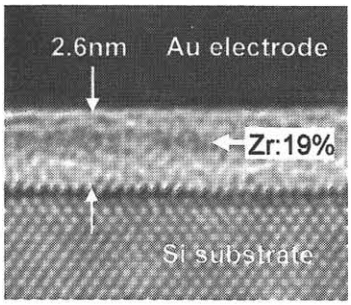

Fig. 5. Cross-sectional TEM image of a 2.6-nm-thick Zr silicate.

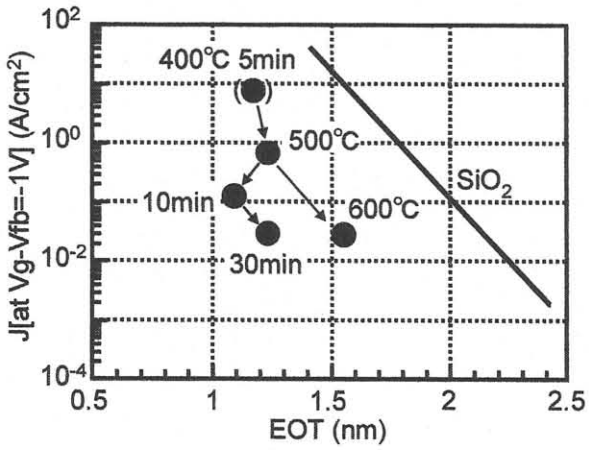

Fig. 7. EOT vs Jg characteristics of ultrathin Zr silicates treated under various PDA conditions.

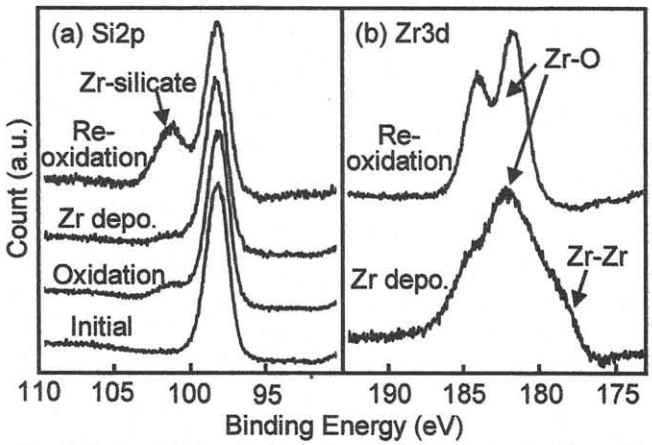

Fig. 2. *In-situ* XPS analysis during fabrication of a Zr silicate film. (a) and (b) show Si2p and Zr3d core-level spectra, respectively.

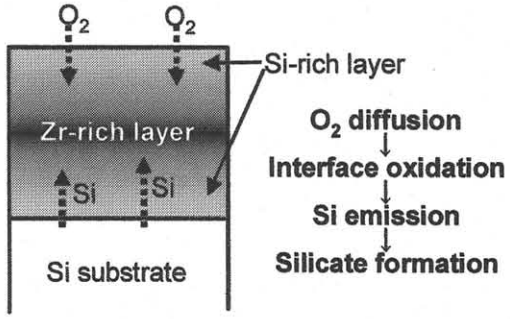

Fig. 4. Schematic illustration of interfacial reactions causing compositional gradation in the silicate.

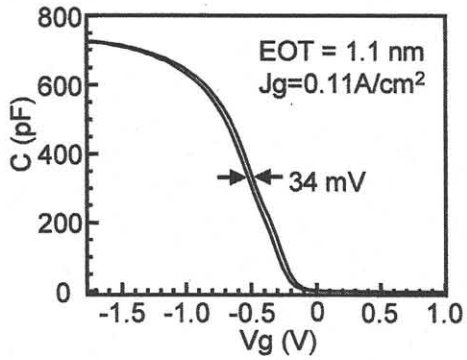

Fig. 6. Typical C-V curve obtained from an ultrathin Zr silicate.

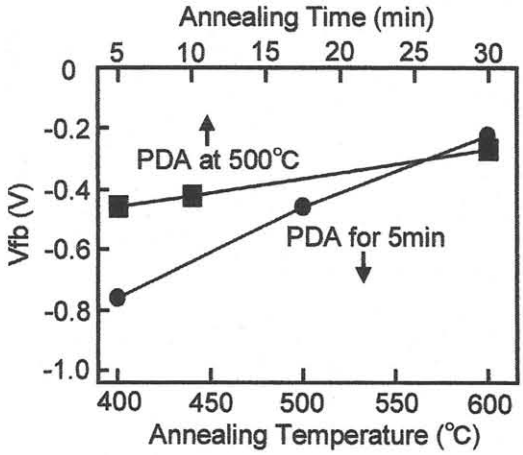

Fig. 8. Changes in Vfb shift under various PDA conditions.