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Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation

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1. Introduction

Thin-body devices, in their double-gate FinFET form[1], and single-gate fully depleted silicon on insulator (FDSOI) form[2] have been demonstrated to have better scalability than traditional bulk transistors. Thus these device architectures are appealing for use in the sub-30nm gate length regime. Although the threshold voltage in thin-body devices can still be controlled with the use of poly-silicon gates and body doping a more attractive method for V_t control is the use of a metal gate with a tunable workfunction. Such an approach allows the body to remain nominally undoped, increasing the carrier mobility and device performance. In this work we demonstrate the fabrication of undoped body metal-gate FinFETs. These devices use NiSi as the gate metal, integrated into the device structure using total gate silicidation (TGS)[3]. V_t was adjusted using a novel dopant segregation technique that allows the tuning of the apparent NiSi workfunction(Φ_m) around the mid-gap energy of Si[4,5].

Poly-Si gated undoped body FinFETs were also fabricated as control devices with identical process conditions to the metal-gate FinFETs. In addition long channel single gate devices with various levels of phosphorous doping were fully silicided to study the how dopants in the gate effect the apparent silicide workfunction.

2. Fabrication Process

The fabrication of the silicide-gate FinFET is shown schematically in Figure 1. FinFET fabrication started with 65 nm Si thick SOI wafers. The fins were patterned lithographically, and transferred to the Si layer with a dry etch. Prior to the 1.6 nm gate oxide the surface of the fin was repaired using a sacrificial oxidation. The gate stack consisted of a 150nm poly-Si gate, which was implanted prior to patterning with boron for pFETs and phosphorous for nFETs. Following gate lithography and etch, the fins were implanted at a high tilt angle in order to uniformly dope the extension regions. Each side of the fin was doped with a separate implant. A nitride spacer was deposited and etched after the extension implants. Spacer was over-etched by 65 nm in order to clear the sides of the fin from nitride. Following spacer formation devices were annealed and a raised source/drain (RSD) was grown using selective silicon epitaxy.

The RSD regions were implanted with zero tilt implants, and then activated with a high temperature rapid thermal anneal (RTA). The first silicidation was performed on the source/drain and gate using a thin layer of Co. The thickness of the cobalt was set so that approximately half of the raised source/drain was silicided. The device was then capped with a 50 nm thick layer of nitride, and subject to a chemical mechanical polishing (CMP) process. CMP was used to expose the tops of the gates by removing the nitride deposited on them. After the gate poly-Si was exposed with CMP the total gate silicidation(TGS) step was performed, transforming the gate from poly-Si to NiSi. The remainder of the protective nitride layer was then etched off and the devices were annealed in forming gas. The portion of the fin under the gate was left undoped through the entire fabrication process.

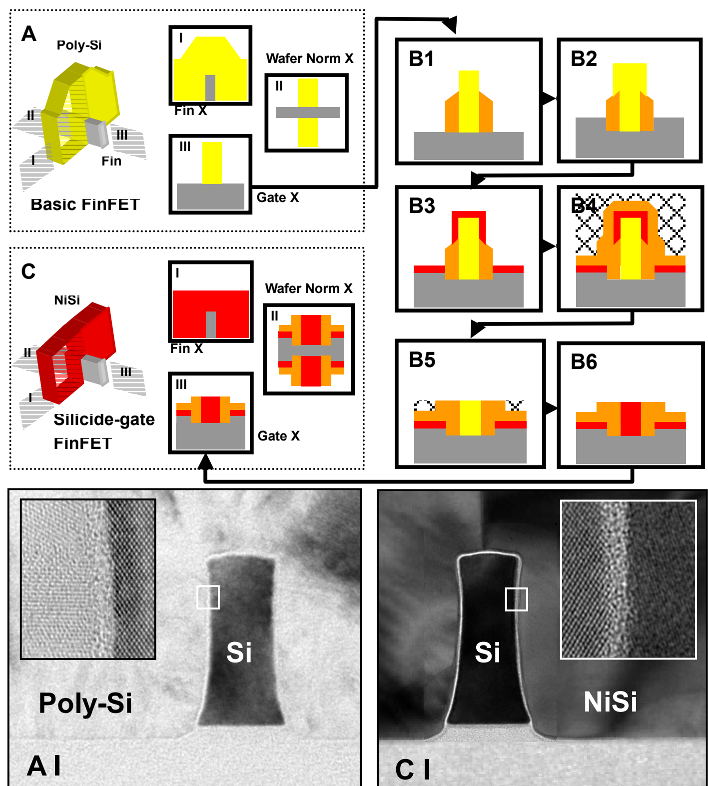

Fig. 1 Process flow used in the fabrication of the metal-gate FinFETs. (A) shows the cross sections of the device after gate etch. (B1-B6) shows the spacer formation, RSD, source/drain silicide, liner deposition, gate CMP, and gate silicide. The two TEM x-sections show are taken from before the gate etch (A I) and after the gate silicide (C I). Insets show zoom of gate oxide.

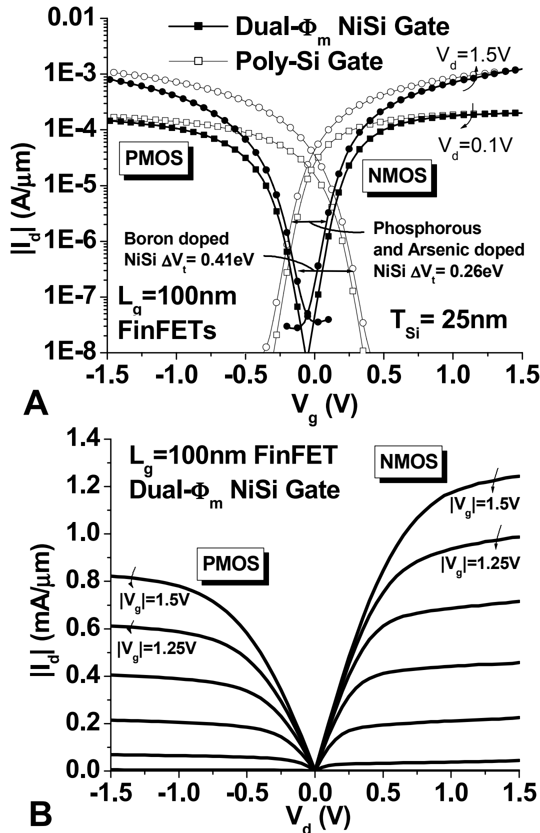

Fig. 2 Electrical characteristics of metal gate FinFETs fabricated through total gate silicidation of doped poly-Si.

3. Electrical Data

The I_d-V_g data for NiSi gated FinFETs with a gate length of 100 nm and fin thickness of 25 nm is shown in Fig. 2a. Also shown are the characteristics of the poly-Si devices with the same dimensions. Subthreshold swing and DIBL are not significantly changed by the presence of the metal gate. Fig. 2b shows the I_d-V_g of the NiSi gated FinFETs. The fins were formed on a (110) surface thus the ratio between NMOS and PMOS performance is smaller then one expected on the traditional (100) surface.

The change in V_t between the poly-Si and NiSi gated FinFETs reflects the difference in the apparent gate workfunction(Φ_m) of the two devices. The NMOS NiSi has the Φ_m of 0.26eV below the n-poly Φ_m while the PMOS NiSi has a Φ_m 0.41eV above the p-poly Φ_m or approximately 0.69eV below the n-poly Φ_m. These two workfuctions were achieved by appropriately controlling the gate doping prior to the silicidation[4,5].

However because workfunction control is a new and highly desirable result the authors have carefully considered alternative explanations and run multiple additional experiments to better understand this effect. There are several parasitic effects that may lead to similar results without resorting to change in workfunction. The two that would produce a similar signature are: incomplete silicidation and dopant diffusion from the gate to the body. Incomplete silicidation is unlikely because in most geometries it would distort the transconductance, but no such distortion is observed. Dopant diffusion is unlikely because the only difference between the control FinFET and the metal gate FinFET is the CMP and gate silicidation, which have a maximum process temperature of 450C, too low for significant diffusion.

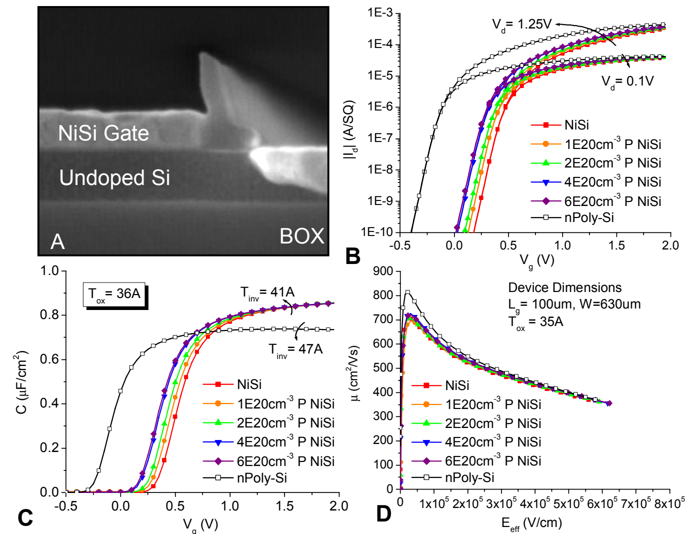

Fig. 3 (A) SEM of the single gate device. (B) IV, (C) CV, (D) mobility for NiSi gated FDSOI nFETs formed on poly-Si doped to various levels with phosphorous (average concentration given).

4. Effect of phosphorous in NiSi

To further understand the effect of phosphorous in NiSi, long channel fully depleted SOI(FDSOI) devices with undoped bodies and NiSi gates were fabricated with varying amounts of gate phosphorous present. Fig.3a shows the SEM cross-section FDSOI device of the device. Fig. 3b,c,d show the I_d-V_g, C_g-V_g, and mobility characteristics respectively, for gates with varying degrees of phosphorous doping. Poly-Si gated controls are also shown. The shift with phosphorous is smaller than seen with both phosphorous and arsenic used in the FinFET. Here the parasitic effects discussed previously can be eliminated as the cause of the V_t shift. Incomplete silicidation can be eliminated through physical analysis, and dopant penetration should cause changes in the shape of the CV and differences in the calculated mobility curves. Neither of these effects is observed.

5. Conclusions

Metal-gate FinFETs offer high gate capacitance and superior mobility, yielding high performance. Dopants in the gate can be used to adjust the V_t without body doping.

References

[1] D. Hisamoto, et al., *IEDM 1998*, p. 1032-1034, 1998
[2] R. Chau et al., *IEDM 2001*, p. 621-624, 2001
[3] B. Tavel, et al., *IEDM 2001*, p. 825-828, 2001
[4] J. Kedzierski, et al., *IEDM 2002*, p. 247-250, 2002
[5] M. Qin, et al., *J Elect.-chem. Soc.,* V. 148(5), p. G271