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A HfAlOx Gate Dielectric FET Technology Compatible with a Conventional Poly-Si Gate CMOS Process

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1. Introduction

A HfAlOx film is one of the promising candidates for high-k gate dielectric applied to 65 nm technology node CMOS, because of the high crystallization temperature (≧ 1050ºC) and its moderate dielectric constant[1]. Integrating a high-k gate dielectric into the conventional CMOS process, and large impurity penetration from a poly-Si gate are considered to be the critical issues. Recently, nitrogen incorporation into high-k films or the SiN cap layer were proposed to overcome this issue [2][3]. However, these counter measures make the gate stack process more complicated. By using a SiON interfacial layer and optimizing post deposition annealing (PDA) after high-k ALD deposition, we have successfully suppressed the gate depletion.

In this paper, we report the CMOS performance of fabricated poly-Si/HfAlOx/SiON gate stack FETs. The effects of the oxidation process after gate electrode definition on the gate dielectric will also be discussed.

2. Fabrication Process

HfAlOx gate dielectric FETs were fabricated on 300mm wafers by a conventional CMOS process as shown in Table 1. After STI and n/p-well formations, a nitrided interfacial layer (SiON) was intentionally formed by NH_3 nitridation and oxidation. A film of HfAlOx with 23% Hf (typically 3 nm thickness) was deposited by ALD at 300ºC, followed by post-deposition annealing. A 150 nm-thick poly-Si film was deposited, followed by n/p-gate implantations. Poly-Si gate electrodes were defined by RIE. The HfAlOx and SiON films were removed by wet etching in order to form shallow S/D extensions by a low energy implantation. The exposed Si substrate surface and poly-Si sidewalls were covered with a 2 nm-thick SiO_2 film formed by CVD-TEOS at 650ºC or by thermal oxidation at 800ºC or 1000ºC. After S/D extension and halo implantations, a SiN sidewall was formed followed by deep S/D implantations. Implanted impurities were activated by a spike annealing at 1050ºC.

The thickness of the HfAlOx film determined by TEM was 2.9 nm, and while the thickness of the SiON film was 0.8 nm, (Fig. 1). The physical thickness of the IFL was kept to less than 1 nm even after the 1050ºC thermal budget. From the relationship between the physical thickness of the HfAlOx film and the EOT obtained from C-V measurements as shown in Fig. 2, the dielectric constant of the HfAlOx film was 17, and the electrical thickness of the SiON was 0.8nm. Fig. 3 is a TEM photograph showing the cross-section of a FET with L_{gate}=70 nm.

3. Results and Discussions

Gate Dielectric integrity

When a conventional CMOS process such as a poly-Si gate electrode is used to fabricate HfAlOx/SiO_2 gate dielectric FETs with impurity activation in gate electrodes and S/D at 1050ºC, large C-V hysteresis due to trap generation and large C-V shift for a p^+ poly-Si gate electrode capacitor due to boron penetration were observed, as shown in Fig. 4. Figure 5 shows the C-V characteristics of the n- and p-capacitors for the poly-Si/HfAlOx/SiON gate stack with three methods of 2 nm-thick SiO_2 film formations after gate electrode definition. In comparison with those for the poly-Si/HfAlOx/SiO_2 gate stack shown in Fig. 4, C-V hysteresis decreased less than 50 mV due to the nitrided interfacial layer. Depletion of the n-capacitor was suppressed. (CET=EOT+0.7nm) Boron penetration was suppressed, except for the 2 nm-thick SiO_2 film formation at 1000ºC for 5 sec. Figure 6 shows I_g-V_g characteristics for n- and p-capacitors, where the gate electrode fully covered the active area. Gate leakage current of the n- and p-capacitors for the HfAlOx/SiON gate dielectrics (EOT=1.5nm) were lower than those for the SiON (EOT=1.8nm). Especially for the capacitor with TEOS gate sidewall and that with 800ºC-thermal oxide gate sidewall, gate leakage current were three orders of magnitude lower at accumulation bias, and one order of magnitude lower at inversion bias. Figure 7 shows the cumulative probability of drain leakage current at Vd=±1.2V for the n and pFETs, where the gate electrode was overlapped to S/D. Though the drain leakage current for the FET with TEOS gate sidewall was the lowest, a small drain leakage current with tight distribution over a 300 mm wafer was obtained for that with thermal oxide gate sidewall at 800ºC. The value of 10^{-12} A/μm satisfies LSTP applications [4]. Therefore, the following CMOS performance was evaluated by n and pFETs with the HfAlOx/SiON gate dielectrics (EOT=1.5 nm) fabricated by the thermal oxidation of gate sidewalls at 800ºC.

CMOS Performance

Vth roll-off for both n and pFETs were suppressed down to L_{gate}=70 nm, as shown Fig. 8. Figure 9 shows the subthreshold swing for nFET (L_{gate} =100 nm) of 76 mV/dec, which was almost the same as that of SiON gate dielectrics, was obtained. Since depletion of the pFET was larger than that of nFET, due to the smaller inversion capacitance shown in Fig. 5, the subthreshold swing for pFET was larger than that of nMOS (88 mV/dec). A drain current of 500 μA/um was obtained for n, and 200 μA/um was obtained for pFETs (L_{gate} =100 nm), as shown in Fig. 10.

4. Conclusions

The conventional CMOS process compatibility of a poly-Si/HfAlOx/ SiON gate stack was demonstrated. C-V hysteresis and Boron penetration were successfully suppressed even after 1050ºC activation. We have also shown that thermal oxidation of gate sidewalls can be applied without increasing the EOT and Jg of the gate stack. Well-behaved CMOS performance with L_{gate} =100 nm was obtained with the high-k gate stack technology.

References

[1] K. Torii *et al.*, *Ext. Abs.63rd Autumn Meeting Japan Society of Applied Physics*, p. 742, 2002.
[2] H-S. Jung *et al.*, *Tech. Dig. IEDM*, p. 853, 2002.
[3] Y. Morisaki *et al.*, *Tech. Dig. IEDM*, p. 861, 2002
[4] *International Technology Roadmap for Semiconductors* 2002.

Table 1. Fabrication flow for HfAlOx FETs

- **Shallow Trench Isolation**
- **We ll Channel Ion Implantation**
- **Gate Dielectric**
  - **RTN Nitridation +Oxidation**
  - **ALD HfAlOx**
- **PDA 1050C 1sec**
- **Gate Poly-Si CVD**
- **Gate-Ion Implantation**
- **Gate Electrode difinition**
- **Oxidation or TEOS deposition**
- **Extension – Ion Implantation**
- **Sidewall formation**
- **S / D – Ion Implantation**
- **Annealing (1050C Spike)**
- **Metallization**

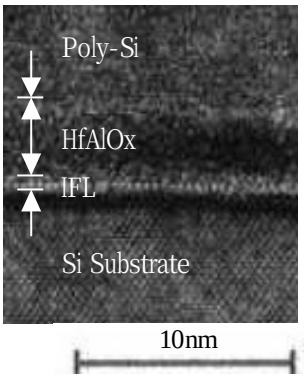

Fig.1 Cross-section TEM image for poly-Si/ HfAlOx/SiON(IFL) gate stack.

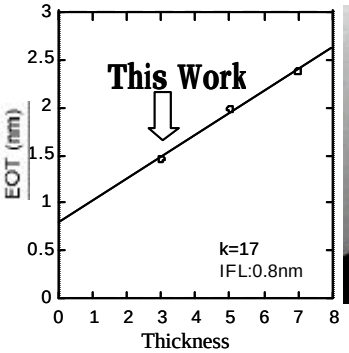

Fig.2 ´Relàtionship between physical thickness of HfAlOx and EOT.

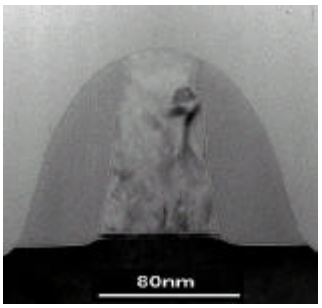

Fig.3 Cross-section TEM image for a HfAlOx FET.

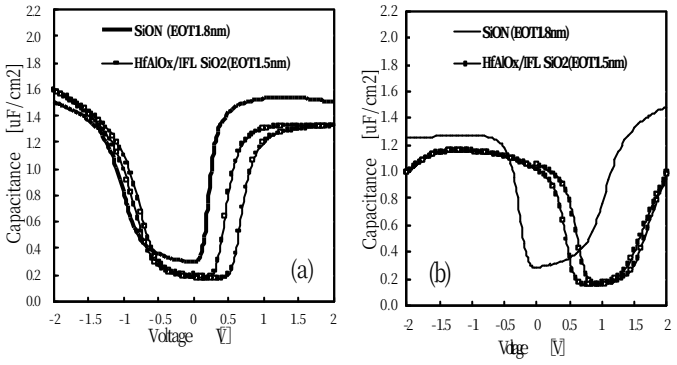

Fig. 4. C-V characteristics of n+ and p+ poly-Si gate capacitors with $HfAlOx/SiO_2$ and SiON (as a reference) gate dielectrics.
(a) n+-poly-Si/p-sub, (b)p +-poly-Si/p-sub

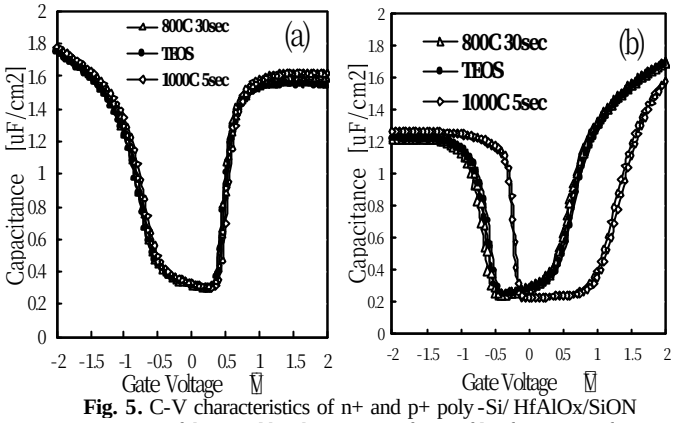

Fig. 5. C-V characteristics of n+ and p+ poly-Si/ HfAlOx/SiON capacitors fabricated by three types of SiO_2 film formation after gate difinition, CVD-TEOS, 800℃ and 1000℃ oxidation.
(a) n+-poly-Si/p-sub, (b)p +-poly-Si/p-sub

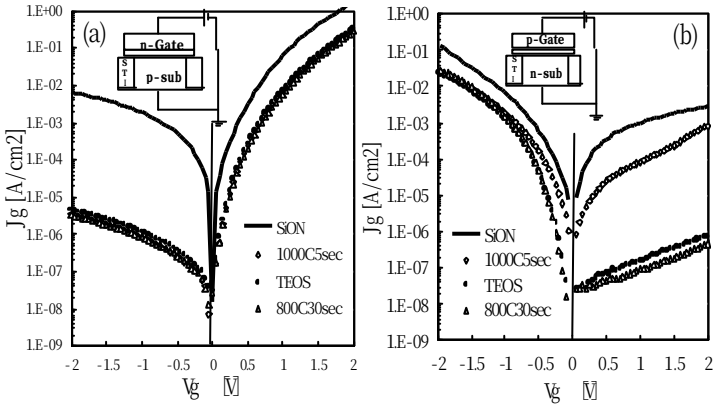

Fig.6 Gate leakage characteristics of n+ and p+ poly-Si/HfAlOx/SiON capacitors. A gate electrode fully covers an active area.
(a) n+ poly-Si/HfAlOx/SiON Capacitor (b) p+ poly-Si/HfAlOx/SiON Capacitor

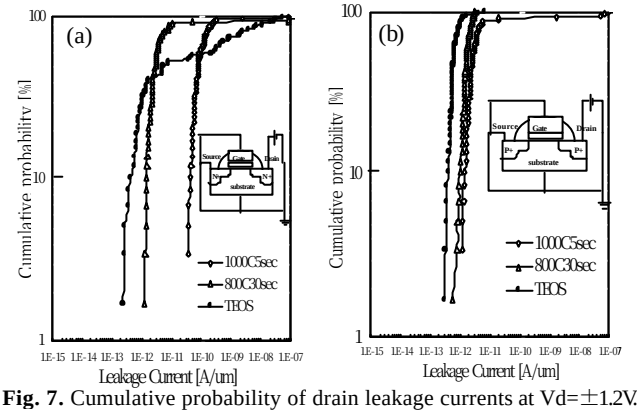

Fig. 7. Cumulative probability of drain leakage currents at Vd=±1.2V.
(a) n+ poly-Si/HfAlOx/SiON FET (b) p+ poly-Si/HfAlOx/SiON FET

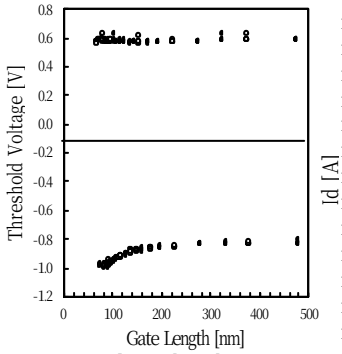

Fig. 8. Relationship between gate poly length and threshold voltage for n and p FETs with HfAlOx /SiON gate dielectric.

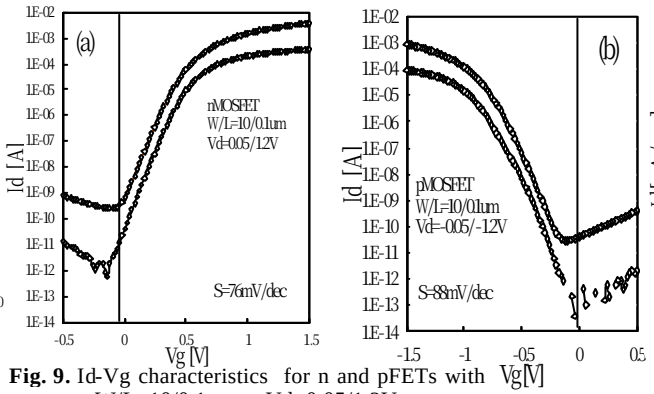

Fig. 9. Id-Vg characteristics for n and pFETs with W/L=10/0.1um at Vd=0.05/1.2V.
(a) n+ poly-Si/HfAlOx/SiON FET (b) p+ poly-Si/HfAlOx/SiON FET

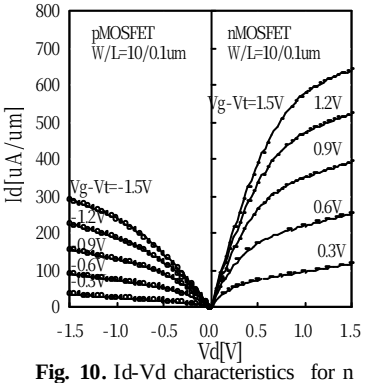

Fig. 10. Id-Vd characteristics for n and pFETs with W/L=10/0.1um at various gate overdrives (Vg-Vt) .