Extended Abstracts of the 2003 International Conference on Solid State Devices and Materials, Tokyo, 2003, pp. 708-709

A-8-1

Schottky Barrier Height Reduction and Drive Current Improvement in Metal Source/Drain MOSFET with Strained-Si Channel

Atsushi Yagishita, Tsu-Jae King[1] and Jeffrey Bokor[1]
Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone: +81-45-770-3662, E-mail: yagishita@amc.toshiba.co.jp
[1] University of California at Berkeley, Department of Electrical Engineering and Computer Sciences
231, Cory Hall #1770, Berkeley, CA 94720-1770, USA

1. Introduction

Schottky Barrier (metal) Source/Drain technology is promising for high-performance nanoscale MOSFETs because it provides shallow and low-resistivity source/drain regions, as well as a simpler fabrication process. The primary challenge for this technology is reduction of the Schottky contact resistance in order to improve transistor drive current. Metal work function control is useful for reducing the contact resistance, but it is insufficient because of the Fermi-level pinning effect [1].

In this paper, we propose to use strain to reduce the Schottky barrier height and hence the contact resistance. As shown in Fig. 1, the energy levels of the 2-fold valley ($\Delta 2$) and 4-fold valley ($\Delta 4$) in the channel are affected by strain, so that the barrier height ($E_{b,\Delta 2}$) for the 2-fold valley can be significantly reduced. The effects of strain and Fermi-level pinning on the Schottky barrier height are first presented, and then the advantages of using a strained-Si channel for the Schottky barrier source/drain MOSFET are described.

2. Simulation model

For simplicity, a 12-nm (gate length) ballistic double-gate transistor structure was used for the device simulations (Fig. 2). The non-equilibrium Green's function method was used to include three carrier emission models at the Schottky contact (Fig. 3) [2]. The Schottky barrier heights for each valley were calculated by using the interface dipole theory and deformation potential parameters to include the strain effect and the Fermi-level pinning effect on the barrier height (E_b).

2-1. Strain effect

Fig. 4 shows the valence- and conduction-band shifts caused by tensile stress (composed of hydrostatic and bi-axial strain components). As shown in this figure, the hydrostatic strain lowers the energy levels of the conduction and valence bands, and the bi-axial strain splits the bands into valleys with different energy levels (2-fold, 4-fold, light hole(lh), heavy hole(hh) and split-off(so)).

2-2. Fermi level pinning effect

According to the interface dipole theory, the metal work function is pinned near the charge neutrality level (E_{cnl}) [3]. The effective metal work function ($E_{m,eff}$) is different from the vacuum work function ($E_{m,vac}$) and can be calculated by using Equation (1) in Table I. The slope parameter S used in the equation was empirically found to be 0.1 in the case of silicon. Therefore, $E_{m,eff}$ is approximately equal to E_{cnl}. E_{cnl} can be calculated by using the cell averaged real space Green's function (Equation (2) in Table I) and silicon energy-band structure [4]. We calculated the silicon energy-band structure by using the empirical pseudo-potential method and included the strain effect in the calculation. Once E_{cnl} is calculated, $E_{m,eff}$ and E_b can be easily obtained.

3. Results and discussion

Fig. 4 shows the calculated E_{cnl} shift caused by strain. It was found that hydrostatic strain changes E_{cnl}, but bi-axial strain has no effect on E_{cnl}. The reason for this result is that E_{cnl} is dependent only on the average level of the conduction band and valence band. It is known that the bi-axial strain splits the band into valleys with different energy levels, but it does not change the average band level. Therefore, E_{cnl} is dependent only on the hydrostatic component. Thus, the Schottky barrier heights for the 2-fold valley ($E_{b,\Delta 2}$) and the light hole valley ($E_{b,lh}$) can be reduced by bi-axial strain without the disturbance of Fermi-level pinning. On the other hand, hydrostatic strain is not useful for reducing E_b due to the Fermi-level pinning. Fig. 5 shows the calculated E_b reduction caused by the strain.

The effect of strain-induced E_b reduction on the performance of the ballistic double-gate MOSFET structure (Fig. 2) was studied next. Fig. 6 shows the typical potential profile (for the first sub-band in the 2-fold valley) in the channel with and without the strain. As indicated in the Figure, E_b is reduced by ~0.1 eV by 1% strain. Fig. 7 shows the strain dependence of the drain current (I_d) and the threshold voltage (V_t). The exponential improvement in drain current with strain is attributable to carrier mobility enhancement and the E_b reduction. Fig. 8 shows the dependence of I_d and V_t on the barrier height (or metal work function, assuming that E_b is determined by $E_{m,vac}$ without any pinning effect). From a comparison of Figures 7(a) and 8, it can be seen that the drain current achieved with 0.015 strain is comparable to that which would be obtained for a device with the zero barrier height (metal work function of 4.05). It should be noted that the bi-axial strain approach to improving I_d is more attractive than the metal work function engineering approach because the strain effect is not disturbed by the pinning effect. However, the sub-threshold slope is degraded by strain (Fig. 9), because the E_b reduction increases the off-state current as well as on-state current (Figures 10 and 11). In order to reduce the off-state current, a thinner Si channel can be used.

4. Conclusions

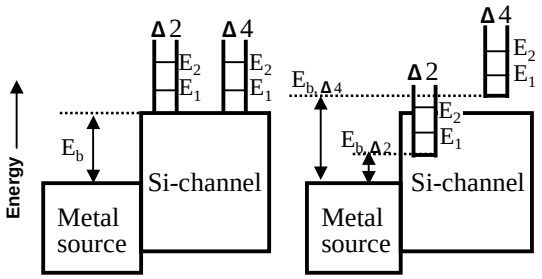
The use of strain to reduce contact resistance and improve the drive current of the Schottky barrier source/drain MOS transistor is proposed. The advantages of this approach were shown by theoretical calculation based on the non-equilibrium Green's function formalism. Furthermore, the interface dipole theory was firstly applied to the calculation in order to clarify the effects of strain and Fermi-level pinning on the Schottky barrier height. The calculated results indicate that bi-axial strain can reduce the Schottky-barrier height and increase CMOS transistor drive current without disturbance of Fermi-level pinning, whereas hydrostatic strain has no effect on the barrier height because of the pinning. These results indicate the combination of the metal source/drain structure with a bi-axially strained Si channel can be beneficial for improving the drive current of nanoscale MOSFETs.

Acknowledgements

We would like to thank Prof. Mark Lundstrom, Dr. Jing Guo, Dr. Yang-Kyu Choi, Mr. Daewon Ha, and Mr. Hideki Takeuchi for valuable discussions and support. We are also grateful to Dr. Kinya Usuda, Dr. Yoshitaka Tsunashima, and Dr. Kyoichi Suguro for their encouragement throughout this work.

References

[1] Jakub Kedzierski *et al.*, *IEDM Techincal Digest*, p.57 (2000)
[2] Jing Guo *et al.*, *IEEE Transactions on Electron Devices*, p.1897 (2002)
[3] Yee-Chia Yeo *et al.*, *IEEE Electron Device Letters*, Vol. 23, p.342 (2002)
[4] C. Ohler *et al.*, *Physical Review B*, Vol. 58, p.7864 (1998)



(a) Relaxed Si (b) Strained-Si

Fig.1 Schematic diagram of energy band structure. (a) Relaxed Si (b) Strained Si

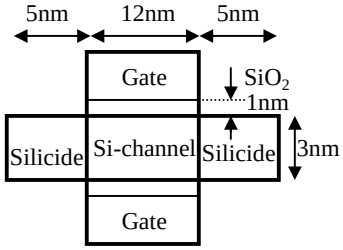


Fig.2 Device structure: Ballistic double-gate MOSFET

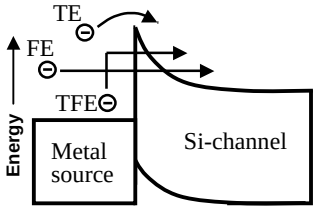


Fig.3 Emission models included in the simulation; TE: thermionic emission, FE: field emission, TFE: thermionic field emission

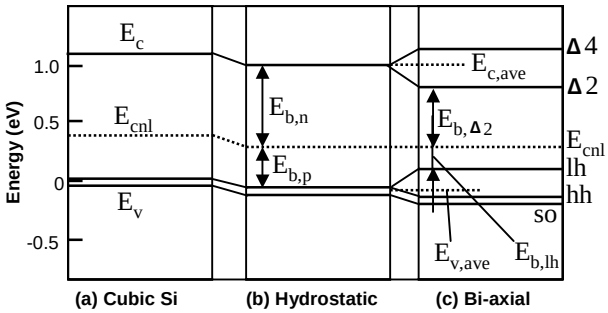


Fig.4 Schematic diagram of energy band structure under tensile strain (E_{xx}=0.02). (a) Cubic Si, (b) Hydrostatic strain component, (c) Bi-axial strain component

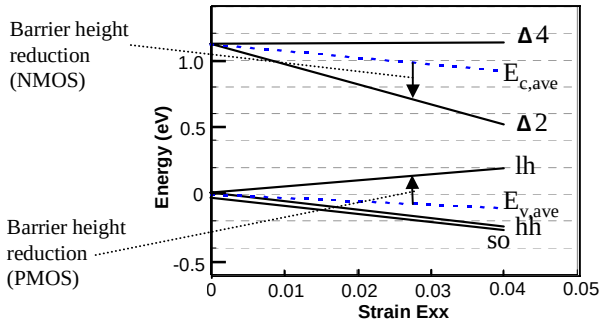
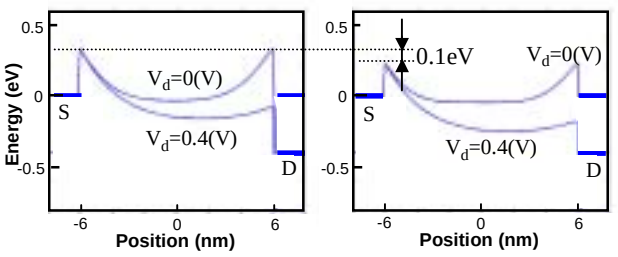
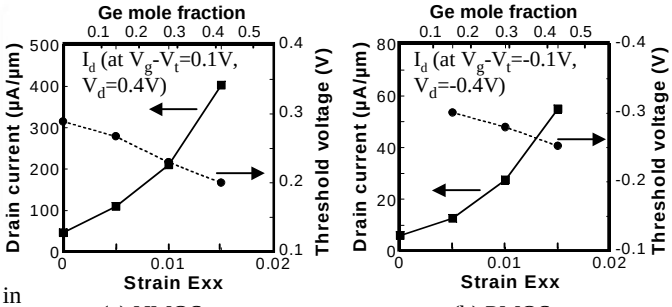


Fig.5 Barrier height reduction caused by bi-axial tensile strain (calculated results)



(a) Relaxed Si (b) Strained-Si

Fig.6 Potential profile in the NMOS channel (first sub-band E_1 in Δ2 Valley). V_g = 0.4V, $E_{c,ave} - E_{m,eff}$ = 0.28eV. (a) Relaxed Si (b) Strained Si, E_{xx} = 0.01



(a) NMOS (b) PMOS

Fig.7 Drain current vs. strain for (a) NMOS and (b) PMOS. (Calculation includes the Fermi-level pinning effect.)

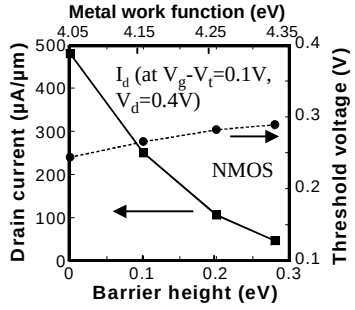


Fig.8 Drain current vs. barrier height. The barrier height is assumed to be adjustable by changing the metal (source) work function, without the pinning effect.

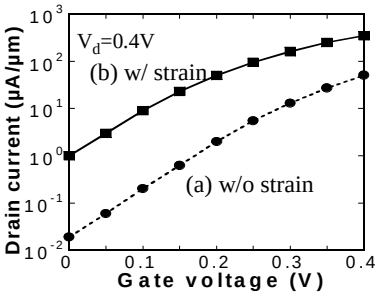


Fig.10 Drain current vs. gate voltage characteristics (NMOS). (a) Relaxed Si, (b) Strained Si, E_{xx}=0.01

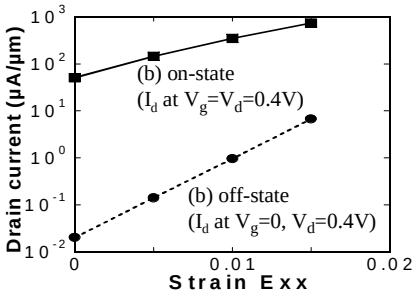


Fig.11 Drain current vs. strain characteristics (NMOS). (a) off-state current, (b) on-state current

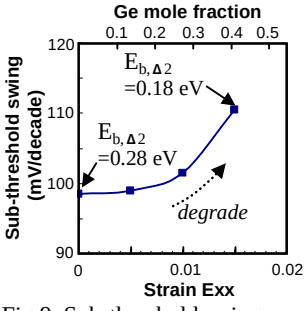


Fig.9 Sub-threshold swing vs. strain (NMOS).

Table I: Equations used for simulations

$E_{m,eff}$: effective metal work function
$E_{m,vac}$: vacuum metal work function
E_{cnl}: charge neutrality level
S: slope parameter
Ψ_{nk}: wave function of Bloch wave vector k and band index n
E_{nk}: energy of the Bloch state
R: lattice vector
g: real space Green's function
G: cell averaged Green's function
G_c: Green's function for conduction band
G_v: Green's function for valence band

Fermi level pinning:

$$E_{m,eff} = E_{cnl} + S \times (E_{m,vac} - E_{cnl}) \quad (1)$$

Real space Green's function:

$$g(r,r',E) = \sum_{nk} \frac{\psi^*_{nk}(r) \cdot \psi_{nk}(r')}{E - E_{nk}}$$

Cell-averaged real space Green's function:

$$G(R,E) \equiv \int dr \cdot g(r, r+R, E) = \sum_{nk} \frac{\exp(ik \cdot R)}{E - E_{nk}}$$

$$|G_C(R, E_{cnl})| = |G_V(R, E_{cnl})| \quad (2)$$