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Halo and LDD Engineering for Multiple V_T High Performance Analog Devices in 0.13μm CMOS Technology

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Abstract

High performance analog (HPA) CMOS devices with multiple threshold voltages have been successfully fabricated by 0.13μm logic based mixed-signal CMOS process in a single chip, that's high-speed digital and analog simultaneously realized by fully CMOS solution. The HPA devices demonstrate superior drivability, DC gain, matching, and reliability by optimized halo and LDD engineering and a unique dual gate oxide module for aggressive oxide thickness scaling to realize analog performance and maintain promisingly good reliability in all aspects.

I. Introduction

The scaling of analog CMOS devices is always behind that of digital CMOS devices in terms of gate length (L_g), gate oxide thickness (T_{OX}), junction depth (X_j), threshold voltage (V_T), and supply voltage (V_{DD}), etc. The limitation comes from the much more stringent requirements for analog devices than standard logic CMOS to assure analog function. The key requirements are the bandwidth (allowed operating frequency), signal swing or dynamic range (DR), linearity, signal-noise-ratio (SNR), power dissipation, and reliability. Unfortunately, inherent trade-off among the device parameters like V_T, G_m (transconductance), G_{DS} (output conductance), DIBL (Drain-Induced Barrier Lowering), SCE (short channel effect), and I_{SUB} (substrate current) generally leads to compromise in the requirements and limits the continuous scaling [1]-[4]. Halo or super-halo engineering has been extensively used to facilitate logic CMOS scaling but is considered to potentially impose penalty on analog devices like reduced early voltage, reduced gain [5]-[6], and degraded reliability. In this paper, we will report multi-V_T analog devices implemented by optimized halo and LDD engineering to achieve lower V_T, larger I_{DSAT}, higher DC gain (G_m/G_{DS}), better matching, and good reliability simultaneously. The lower V_T offers great help on DR. I_{DSAT} is increased by more than 30% and matching is improved by around 42/26~40% for n/p MOS. The DC gain is compromised with I_{DSAT}, SCE and HCI(hot carrier injection) lifetime all together and becomes a tougher issue for nMOS than pMOS. Optimized halo and LDD engineering is proven by obviously higher DC gain than non-halo devices and sufficient HCI lifetime. Superior ESD hardness is one more indicator to justify the halo and LDD engineering as manufacturable process for mixed signal single-chip integration.

II. HPA Device Performance and Reliability

1) Device Performance &Reliability-Halo & LDD Engineering

HPA n/p MOS with standard-V_T (std-V_T) and low-V_T are fabricated on the same chip but separated halo and channel implants to achieve the dramatically different V_T targets. T_{OX} is scaled from 65Å for standard 3.3V IO devices to 50Å for the HPA devices in this study. An elaborated dual gate oxide module has been developed to assure the oxide reliability under over-drive [7]. Table 1 indicates the HPA device performance parameters and comparison with the standard 3.3/2.5V IO respectively. For std-V_T n/p MOS, DR is improved by around 0.2/0.1V attributed to lower V_T (0.37/-0.5V vs. 0.58/-0.6V), I_{DSAT} is boosted by 170/110 μA/μm (around 30%). Regarding low V_T n/p MOS, further gain in DR to around 0.43/0.35V is achieved by relatively lower V_T target and I_{DSAT} is increased by 275/220 μA/μm (around 45/75%). DC gains of 50 is achieve for 0.32μm nMOS while higher gain of 72 is realized for 0.28μm pMOS. The tougher challenge to nMOS in terms of high DC gain comes from the trade-off with SCE and HCI. In this study, DIBL and I_{SUB} are two parameters used to quantify SCE and HCI respectively. Figs.1~2 show the halo implant effect on DC gain and DIBL in which DC gain of 50 and DIBL below 0.1V can be achieved for 0.32μm nMOS by using optimized halo implant. Fig.3 indicates a universal curve of DC gain vs. DIBL for both halo and non-halo devices in which the DC gain of 50 is corresponding to DIBL of around 0.095V. Fig.4 shows one more benefit offered by halo implant to I_{SUB} reduction at the specified DC gain target. We see that I_{SUB} of around 4.6~4.8μA/μm under 1.1V_{DD} (i.e., 10% over-drive at drain) can meet DC gain of 50 for halo nMOS but the DC gain drops to near 30 for non-halo nMOS with the same I_{SUB} level. It indicates that non-halo nMOS suffered poor DC gain due to worse SCE and didn't provide any help on reducing I_{SUB}, i.e. HCI effect. Regarding the LDD engineering as a possible solution to compensate for the trade-off, Fig. 5 demonstrates LDD split (energy and dose) effect on non-halo nMOS in terms of DC gain and I_{SUB}. We see that DC gain above 50 can be achieved for 0.32μm nMOS for split A with ultra-low energy LDD (NLDD A <10kev) but dramatically higher I_{SUB} beyond 5.5μA/μm will degrade the HCI lifetime. Table 2 summarizes the halo and LDD implant effect on I_{SUB} and HCI lifetime with good correspondence. Use of higher LDD energy (NLDD B~D >20kev) really helps to reduce I_{SUB} and improve HCI lifetime (3~3.5yrs) but poor DC gain of around 30 is the penalty as shown in Fig.5. The HCI lifetimes, $\tau_{0.1\%}$ defined by cumulative failure rate at 0.1% are shown in Figs.6~8 corresponding to 3 LDD splits of non-halo nMOS and compared to halo nMOS in Fig.9. We see that $\tau_{0.1\%}$ of the halo nMOS, i.e. 0.55yrs is more than double that of non-halo nMOS with the same DC gain, i.e. 0.24yrs for NLDD A. Regarding halo implant effect on pMOS reliability, NBTI (negative bias temperature instability) is of special concern. Table 3. summarizes the NBTI lifetimes for non-halo and halo pMOS in which all three pMOS pass the spec. of $\tau_{0.1\%}$=5 years. It's noted that P^+ gate implant (incorporating F^+) instead of halo implant presents significant effect on NBTI. The lifetime $\tau_{0.1\%}$ can be improved by more than 3 times, from 41 years to near 150 years. Fig.10 shows the cumulative plot of NBTI lifetimes for non-halo pMOS with splits of P^+ gate implant and Fig.11 shows that of halo pMOS w/o P^+ gate implant. Concerning halo implant impact on nMOS, ESD hardness is one more key item no less important than HCI to be verified. Fig.12 compares the I_{t2} measured by TLPG (transmission line pulse generator) in which halo and non-halo nMOS can pass ESD with sufficient I_{t2} at 3.53 and 3.3A representing HBM/MM of 7KV/350V for halo nMOS and 6.6KV/330V for non-halo nMOS, respectively.

2) Device Matching – Std V_T & Low V_T HPA and standard IO

The importance of device matching in terms of analog circuit

performance and yield has been emphasized [4]. The potential impact caused by Halo implant on mismatch becomes a critical concern to be verified. Table 4 shows the mismatch in terms of Avt-gm and Aidsat representing slope of the standard deviation of V_T and I_{DSAT} mismatch vs. $1/(WL)^{1/2}$. The advantage of HPA 50Å devices featured by obviously less mismatch is identified as compared to standard 50Å IO, that's around 20~23/12~28% and 42/26~40% improvement in terms of Avt-gm and Aidsat for std-V_T n/P MOS respectively. It's noted that low-V_T n/p MOS provide further reduction of mismatch by around 50% that matches with dopant fluctuation theory.

III. Conclusions

Manufacturable logic CMOS based HPA process has been developed for high performance analog applications. The optimized Halo and LDD engineering to ensure V_T and L_g scaling has been proven by excellent performance in terms of drivability, gain, and matching. Besides, promisingly good reliability in all aspects like HCI, NBTI and ESD has been demonstrated simultaneously.

Acknowledgement

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Table 1. HPA device portfolio and comparison with standard 3.3V & 2.5V IO

Device V_T Options	HPA 50A Si				Standard IO Target			
	Std-V_T		Low-V_T		3.3V IO		2.5V IO	
Device Type	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
V_{DD} (v)	3.3		3.3		3.3		2.5	
EOT (A)	50		50		65		50	
$L_{NOM(TEM)}$(μm)	0.32	0.28	0.32	0.28	0.35	0.3	0.24	0.24
V_T@(W=10/L_{NOM})								
V_T@$G_{M,MAX}$	0.41	-0.5	0.21	-0.24	---	---	---	---
V_T@C.C.	0.37	-0.51	0.155	-0.26	0.58	-0.6	0.47	-0.5
I_{DSAT}@V_{DD} (μA/μm)	770	410	874	520	600	300	630	300
$I_{OFF(NOM)}$@V_{DD} (nA/μm)	0.03	0.002	45	2.8	N/A	N/A	N/A	N/A
$I_{OFF(MAX)}$@V_{DD} (nA/μm)	0.135	0.01	93	14.7	0.1	0.1	0.1	0.1
V_T@$G_{M,MAX}$ (W/L=10/10)	0.364	-0.54	0.06	-0.237	---	---	---	---
G_M*R_{DS}@(W=10/L_{NOM})	50	72	41	35	N/A	N/A	N/A	N/A

Table 2. Halo & LDD implant effect on nMOS HCI lifetimes

(LDD energy : A=B< E< C< D, dose : A=B > E >C >D)

Halo	NLDD Splits	I_{DSAT}@ 3.3V (μA/μm)	$I_{SUB,MAX}$@ 3.3V (μA/μm)	$I_{SUB,MAX}$@ 3.6V (μA/μm)	$\tau_{0.1\%}$ (yrs) $1/V_D$ model
x	A	747	2.1	5.62	0.24
x	B	723	2.1	5.69	0.712
x	C	789	1.597	4.25	3.468
x	D	772	1.39	3.74	2.949
v	E	771	1.96	4.89	0.55

Table 3. Halo and P+ gate implant effect on pMOS NBTI

Splits	Halo	P+ gate implant	Sigma	MTTF ($\tau_{50\%}$) (yr)	$\tau_{0.1\%}$ 1.0V_{DD} (yr)
A	x	x	0.1975	41	22.27
B	x	v	0.27557	147	62.73
C	v	x	0.2391	22.25	10.6

Table 4 HPA halo device mismatch and comparison with standard 50A IO

Devices		HPA 50A				50A IO	
		Std-V_T		Low-V_T		Std-V_T	
		NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Avt_gm (mV-um)	x-couple	7.316	4.526	6.69	5.12	9.24	5.99
	parallel	7.479	4.505	7.7	4.68	9.05	5.07
Aidsat (%-um)	x-couple	0.479	0.56	0.43	0.513	0.73	0.87
	parallel	0.479	0.583	0.4	0.513	0.72	0.76

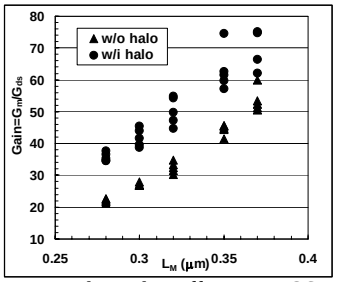

Fig. 1 Halo implant effect on nMOS DC gain vs. drawn gate length (L_M)

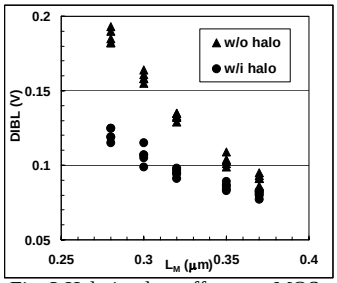

Fig. 2 Halo implant effect on nMOS DIBL vs. drawn gate length (L_M)

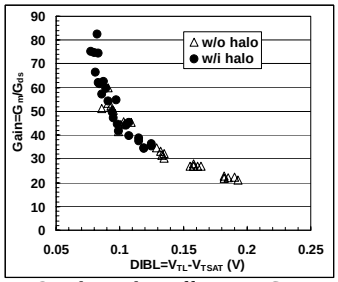

Fig.3 Halo implant effect on DC gain vs. DIBL

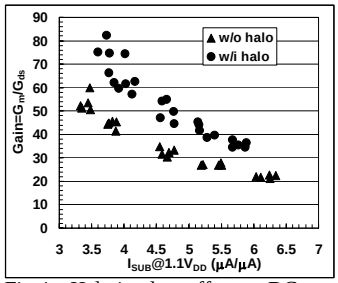

Fig.4 Halo implant effect on DC gain vs. I_{SUB}@1.1VDD

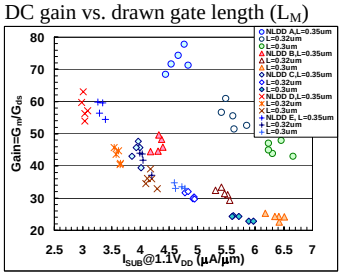

Fig. 5 NLDD effect on non-halo nMOS DC gain vs. I_{SUB}@1.1V_{DD}

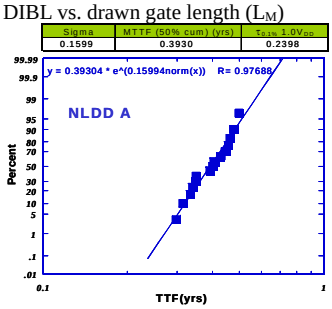

Fig.6 Non-halo NLDD A HC lifetime

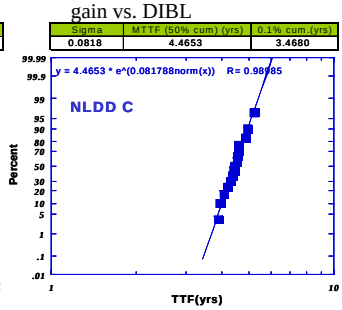

Fig.7 Non-halo NLDD C HC lifetin

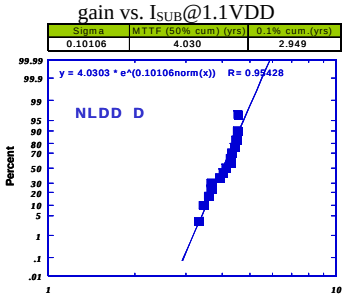

Fig. 8 Non-halo NLDD D HC lifetime

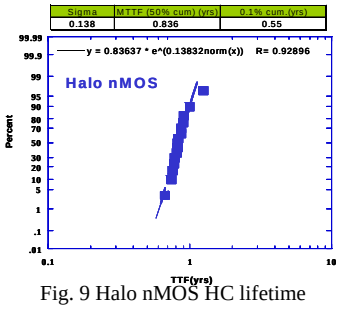

Fig. 9 Halo nMOS HC lifetime

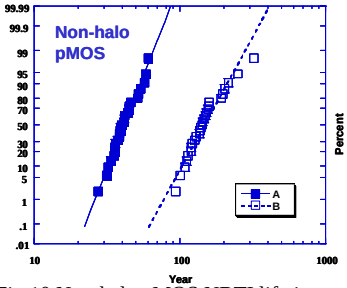

Fig.10 Non-halo pMOS NBTI lifetime

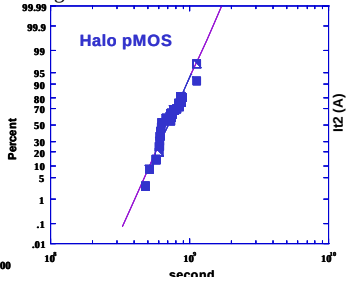

Fig.11 Halo pMOS NBTI lifetime

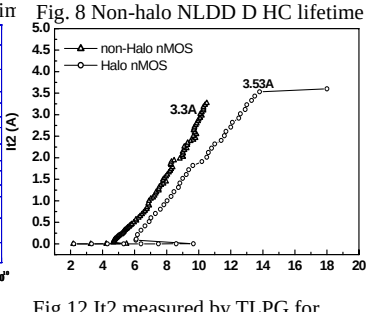

Fig.12 It2 measured by TLPG for halo and non-halo nMOS