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Thermal Stability of Metal Gate Work Functions

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1. Introduction

Metal gate electrodes not only eliminate the gate depletion and dopant penetration problems in CMOS transistors, but also reduce the gate sheet resistance [1]. In selecting metal gate materials, the metal work function Φ_m and its thermal stability is the important consideration since it directly affects the threshold voltage and the performance of a transistor. Integrating metal gate electrodes in a CMOS process is a challenging task since Φ_m is observed to be dependent on the underlying gate dielectric [2,3] and on fabrication process conditions [4-9]. The dependence of Φ_m on the gate dielectric material was explained by Yeo *et al.* [2,3] to be due to dipole formation at the interface of the gate electrode and the gate dielectric. This model is particularly successful for metal-dielectric interfaces where there is minimal interfacial reaction [2,3], or where *intrinsic states* or metal-induced gap states (MIGS) dominate. However, integrating metal gates in a gate-first or conventional approach is very attractive for introducing metal gates in a manufacturable process, and this typically requires the gate-stack to undergo high temperature S/D annealing process. Therefore, the metal/dielectric interface interaction and the dependence of Φ_m on the annealing temperature are critically important and must be clearly understood.

In this paper, we report new experimental findings on the dependence of Φ_m on the underlying gate dielectric materials and process temperature, and present a model to explain the phenomenon of process-induced Φ_m thermal instability. We also show that high temperature annealing could lead to the creation of *extrinsic states*, and hence the interface dipole, at the metal-dielectric interface, resulting in metal Fermi level pinning.

2. Experiment

Capacitors with HfN, TaN, TaTi, and TaTiN metal gates were fabricated. HfN was used as the capping layer on TaN, TaTi, and TaTiN gate electrodes to minimize oxygen diffusion through the gate stack during high-temperature post process, and hence eliminate variation of the equivalent SiO_2 thickness (EOT) of the gate dielectric induced by oxygen diffusion [9,10].

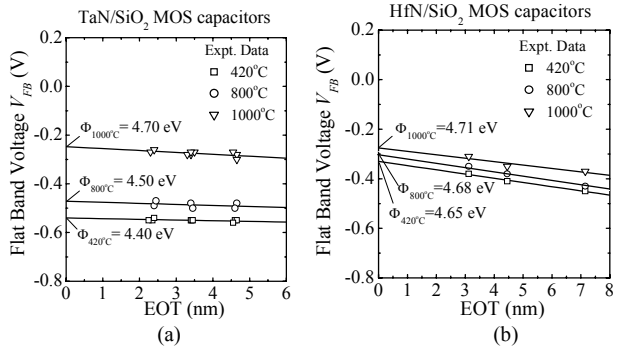

Fig. 1. Flat band voltage V_{FB} versus SiO_2 dielectric thickness after annealing at various temperatures for (a) HfN/TaN/SiO_2/Si and (b) HfN/SiO_2/Si MOS capacitors.

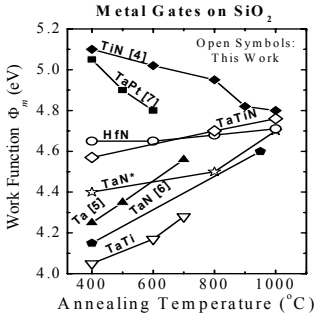

Fig. 2. The variation of metal work function with annealing temper-ature. The gate dielectric is SiO_2.

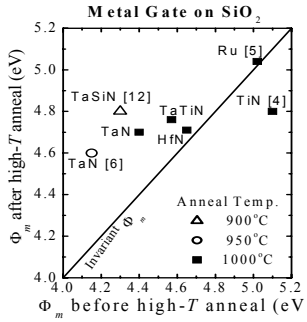

Fig. 3. Impact of high temperature anneal on metal work function on SiO_2.

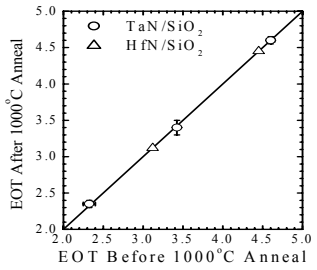

Fig. 4. Gate dielectric EOT does not change significantly after 1000ºC anneal.

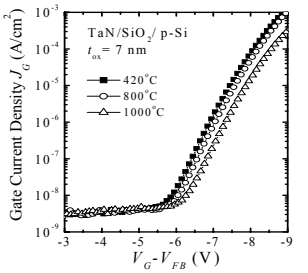

Fig. 5. J_G is reduced with annealing in HfN/TaN/SiO_2/Si due to an increase in Φ_m.

The gate dielectric is thermally grown SiO_2 or CVD HfO_2 with different thicknesses. Details of the fabrication were reported in [10]. To study the thermal stability of Φ_m, the capacitors were annealed in forming gas (N_2/H_2) at 420ºC for 30 min., followed by rapid thermal anneal (RTA) at 800-1000ºC for a duration of ~20 s. Values of Φ_m were extracted from plots of the flat-band voltage V_{fb} versus the gate dielectric EOT.

3. Results and Discussion

Fig. 1 shows the extraction of Φ_m for HfN/TaN/SiO_2 and HfN/SiO_2 capacitors that were annealed at various temperatures. The variation of Φ_m with annealing temperature for various metal gate materials on SiO_2 is summarized in Fig. 2, showing that annealing temperature is a major factor affecting Φ_m. Another way to illustrate the impact of high temperature (high-*T*) anneal is to plot Φ_m before and after annealing on the horizontal and vertical axes, respectively, as shown in Fig. 3. Most data points deviate from the solid invariant line, emphasizing that Φ_m of most metal gates on SiO_2 change considerably upon high-*T* annealing. This change in Φ_m is not attributed to new compounds (metal silicide or high-K) formation at metal/SiO_2 interface [4,9]. In fact, negligible interfacial reaction occurred between TaN or HfN and the SiO_2 gate dielectric, as the EOT of the gate dielectric did not change upon annealing (Fig. 4). For samples where Φ_m is increased after annealing, e.g. HfN/TaN/SiO_2, the gate leakage current density is reduced for a given V_G - V_{fb} due to an increase in barrier height (Fig.5).

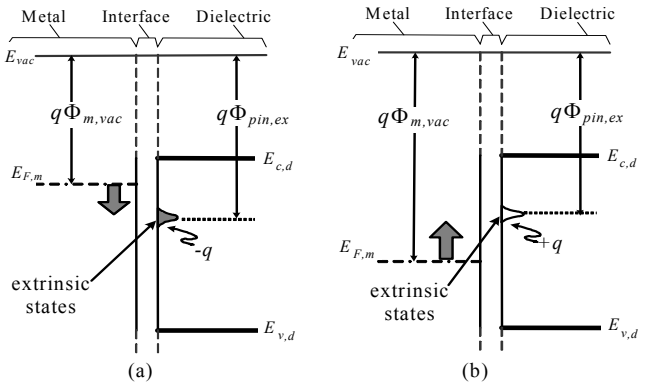

Fig. 6. Schematic of energy band diagram for a metal gate on a dielectric, showing extrinsic states that affect the metals with Fermi level $E_{f,m}$ (a) above or (b) below the pinning level.

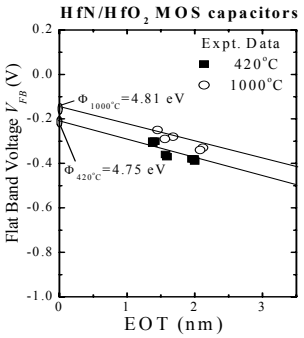

Fig. 7. Plot of V_{fb} versus EOT of HfN/HfO_2/Si MOS capacitors before and after 1000°C anneal.

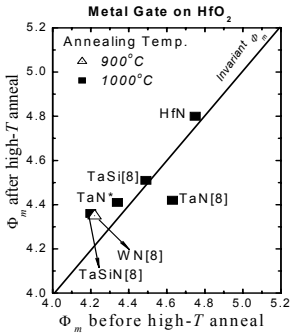

Fig. 8. Impact of high temperature anneal on metal work function on HfO_2. (data TaN* from this work)

It is known that when the gate dielectric is SiO_2, *intrinsic states* at the metal-SiO_2 interface do not significantly modify the vacuum work function of the metal [3]. The change in Φ_m with increasing temperature is therefore predominantly attributed to extrinsic states. In Fig. 2, a notable trend is that Φ_m of metals like TiN, Ta, TaTi, TaN, TaPt, TaTiN, and HfN converge as the annealing temperature is increased. This is likely to be due to the creation of a high density of localized extrinsic states at about 4.7-4.8 eV below the vacuum level (Fig. 6). Extrinsic states, usually associated with bonding defects, leads to Fermi pinning and the convergence of Φ_m. Given the chemical similarity of Ti, Hf and Ta, it is plausible that gates containing these metals form extrinsic states with similar characteristics at the interface with SiO_2. The extent of Fermi pinning due to extrinsic states increases with increasing annealing temperature. Elevation of the annealing temperature probably increases the density of extrinsic states and their effectiveness in pinning the Fermi level of the metal gate.

Fig. 6 shows our model for a metal-dielectric interface where interface dipole induced by extrinsic states contributes to Fermi pinning. When the metal Fermi level $E_{f,m}$ is above the energy level of the extrinsic states [Fig. 6(a)], empty states at the pinning location (at an energy $q\Phi_{pin,ex}$ below the vacuum level) are filled with electrons from the metal and are charged negatively on the dielectric side, driving $E_{f,m}$ towards the pinning level. When $E_{f,m}$ is below the energy level of the extrinsic states [Fig. 6(b)], the extrinsic states are positively charged, also driving $E_{f,m}$ towards the pinning level. The Fermi pinning effect will be less pronounced for metals with $E_{f,m}$ close to the pinning level of the extrinsic states.

The position of the pinning level $q\Phi_{pin,ex}$ with respect to the vacuum level could be related to the interfacial bonding defects between the gate electrode and gate dielectric, and is determined by both the gate electrode and the gate dielectric materials. Pinning levels induced by Hf-Si and Al-O-Si bonds have been reported for poly-Si/HfO_2 and poly-Si/Al_2O_3 interfaces, respectively [11], but not for the metal-SiO_2 interface. It should be noted that the change in Φ_m caused by extrinsic states is not a universal phenomenon that occurs for all combinations of metal gates and gate dielectrics. For example, Φ_m of HfN, Ru [5] on SiO_2 changes little with annealing. This could be possibly due to the absence of extrinsic states at the associated interfaces or, for the case of HfN, the close alignment between the $E_{f,m}$ and the Fermi pinning level.

The value of Φ_m on HfO_2 is considerably determined by intrinsic states or MIGS even before high temperature annealing. Fig. 7 shows the extraction of Φ_m for HfN/HfO_2 capacitors after various thermal treatments. A similar Φ_m extraction is performed for HfN/TaN/HfO_2 capacitors. The values of Φ_m before and after high-T anneal are plotted in Fig. 8. We observed that the work function of a metal such as TaN or TaSiN appears to be more thermally stable on HfO_2 than on SiO_2. This is possibly due to two reasons. Firstly, intrinsic states at the metal-HfO_2 interface already have a significant effect on the modification of Φ_m [2,3], and the role of extrinsic states is comparatively diminished. Secondly, it could be possible that the creation of extrinsic states or interfacial bonding defects at the TaN-HfO_2 or TaSiN-HfO_2 interface is not significant upon thermal annealing. The likelihood of extrinsic states generation could be determined by the chemical constituents in the gate dielectric and the gate electrode. For example, given the similarity in atomic radii and electronegativity of metal atoms in the metal gate and the metal atoms in the high-K gate dielectric, it is plausible that chemical reactions are less likely to occur at the metal-HfO_2 interface than at the metal-SiO_2 interface [8].

4. Conclusion

The dependence of Φ_m on annealing temperature was investigated. A metal-dielectric interface model that takes the role of localized extrinsic states into account was proposed to qualitatively explain the Φ_m instability phenomenon. The creation of extrinsic states and the resulting Fermi level pinning of Φ_m is observed for several combinations of metal gate and gate dielectric materials. The effect appears to be thermodynamically driven, becoming more pronounced when the annealing temperature is higher. Interface dipole formation plays an important role in determining the amount of Fermi pinning and the threshold voltage of metal gate transistors.

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References: [1] ITRS, 2003.(http://public.itrs.net). [2] Y.-C. Yeo *et al.*, *IEEE EDL*, v.23, p.342, 2002. [3] Y.-C. Yeo *et. al.*, *JAP*, v.92, pp. 7266, 2002. [4] J. Westlinder *et. al.*, *IEEE EDL*, v.24, p.550, 2003. [5] J. Lee *et. al.*, *IEDM*, 2002, p.359. [6] C. S. Kang *et. al.*, *JVST-B*, v.21, p.2026, 2003. [7] B. Y. Tsui *et al.*, *IEEE EDL,* v.24, pp. 153, 2003. [8] J. K. Schaeffer *et. al.*, *JVST-B*, v.21, p.11, 2003. [9] C. Ren *et. al.*, *IEEE EDL,* v.25, p.123, 2004. [10] H. Y. Yu *et. al.*, *IEDM,* 2003, p.99. [11] C. Hobbs *et. al.*, *VLSI Tech. Dig.,* 2003, p.9. [12] Y. S. Suh *et. al.*, *IEEE EDL*, v.24, p.439, 2003.