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Etch-byproduct Pore Sealing for ALD-TaN Deposition on Porous Low-k Film

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1. Introduction

The interconnect propagation delay has to be shortened for ULSI devices to operate at higher speeds. The time constant of the delay is a product of the interconnect resistance and inter-dielectric capacitance; therefore, the delay can be reduced by lowering the interconnect resistance and inter-dielectric capacitance. An ultra-thin barrier metal film deposited by atomic layer deposition (ALD) and a low dielectric constant (low-k) material with pores can reduce the resistance of Cu interconnects and the inter-dielectric capacitance, respectively, and these are being considered as interconnect materials for the next generation of ULSIs.

However, the deposition of ALD barrier metals on porous low-k materials results in precursors penetration into the pores. This penetration degrades the electrical performance through increased leakage current. There are a few methods reported to prevent such penetration [1]. We have investigated the pore sealing by CVD method. Figure 1 shows the properties of two level Cu and porous **m**ethyl-**s**ilse-**q**uioxane type porous low-k (p-MSQ) single damascene interconnects with ALD-TaN (1 nm) barrier metal and CVD-SiC pore sealing. The interconnect structure of ALD-TaN barrier and the CVD pore-sealing result in a low via resistance with no penetration, and thus will be used as reference in this article.

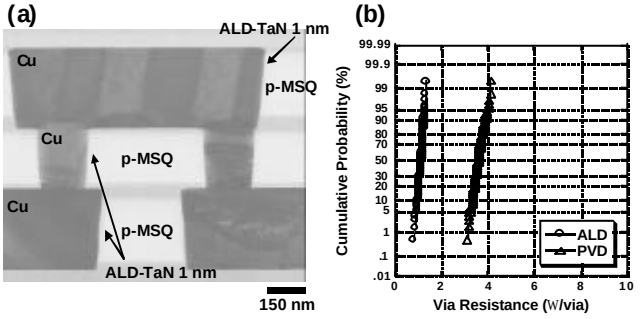

Fig. 1 (a) XTEM pictures and (b) cumulative probability of the via resistance of 50k via chains (M1=M2=ϕ=0.16 μm) for Cu/p-MSQ single damascene interconnects with ALD-TaN (1 nm) and CVD-SiC pore sealing (reference structure in this article).

One issue regarding the CVD pore-sealing method is an increase of process steps. We have investigated the relationship between penetration and pore sealing to develop a novel pore-sealing method by etch-byproduct technique which does not increase the number of process steps.

2. Experimental

A p-MSQ film with a dielectric constant of 2.4 was used as the low-k material. Porosity and pore size (the most distributed) of the p-MSQ was 31% and 1.51 nm, respectively, as measured by high-resolution specula X-ray reflectivity (SXR). SiO_2 (150 nm)/p-MSQ (250 nm) deposited on an SiC stopping layer (50 nm) were patterned into a trench shape by using a photo resist mask. Two kinds of the patterning wafers were prepared to compare the penetration into the low-k film; one is a post resist-stripping sample and the other is a post stopper-etching. ALD-TaN (1 nm) was deposited by cycle exposure of **p**entakis-**d**i-**m**ethyl-**a**mino-**t**antalum (PDMAT)/Ar/NH_3/Ar on these substrates. Cu was electro-chemically filled in the trench, and the samples were annealed at 350°C for 30 min in N_2/H_2 ambient.

Two kinds of low-k capping layer, with and without SiC, were used in the pore sealing by etch-byproduct method. The structures were SiC (50 nm)/SiO_2 (100 nm) and SiO_2 (150 nm), respectively. They were deposited on p-MSQ (250 nm)/SiC (50 nm), after which photo resist mask patterning was carried out. Cu was electro-chemically filled in the trench followed by the annealing.

Penetration of Ta into the low-k material was observed by transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDX).

3. Results and Discussions

Ta Penetration into Low-k

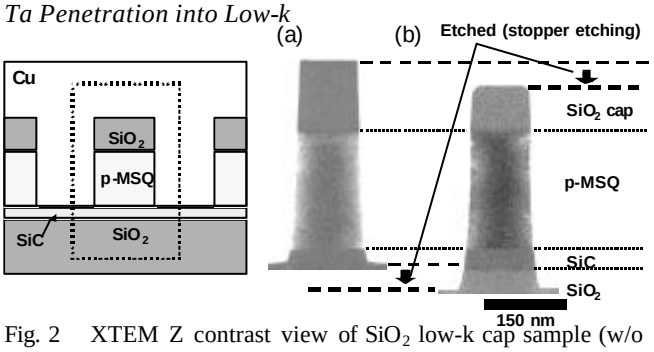

Fig. 2 XTEM Z contrast view of SiO_2 low-k cap sample (w/o SiC cap). ALD-TaN was deposited after (a) resist stripping and (b) stopper etching. The bright dots in the Z-contrast view indicate heavy atoms.

Figure 2 shows the Z-contrast view of TEM cross-sections; ALD-TaN was deposited after (a) resist stripping and (b) stopper etching. The bright dots in the pictures indicate heavy atoms. Therefore, bright regions in

the p-MSQ indicate metal penetration. TaN-ALD after resist-stripping resulted in larger penetration than after stopper-etching. Stopper etching had a sealing effect against penetration. Our further investigation revealed this improvement depends on the stopper-etching conditions.

Typical EDX curves from the p-MSQ are plotted in Fig. 3. Not only a Ta peak, which is due to the PDMAT penetration, but also Cu peaks appear in the EDX curve from the penetrated region. ALD-TaN (1 nm) was reported to prevent Cu diffusion up to 600°C in the case of a SiO_2 substrate [2]. Therefore, Cu should not diffuse into the p-MSQ through the ALD-TaN 1 nm. However, the thickness of the ALD-TaN at the some of the pores should be much thinner, and some of them should be completely open. Cu penetration was probably occurred by the Cu diffusion into the p-MSQ through such pores (Fig. 4).

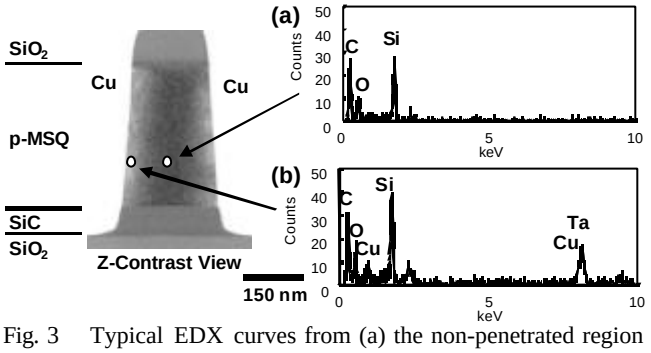

Fig. 3 Typical EDX curves from (a) the non-penetrated region in the p-MSQ and (b) the penetrated region.

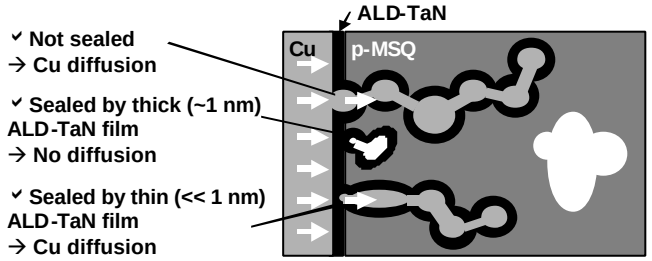

Fig. 4 Cross section of Cu/ALD-TaN/p-MSQ interface.

Electrical Results for Etch-Byproduct Method

Figure 5 shows cross sections of a p-MSQ trench with and without SiC low-k cap by TEM. The sample without SiC cap had no observable etch-byproduct and resulted in the metal penetration. While the sample with SiC cap, which had etch-byproducts at the sidewall, successfully prevented the penetration.

In the case of the 'without SiC cap', XPS data revealed that the etch-byproduct was mainly –CF– based material. The higher sealing ability of the post stopper-etching sample compared with the post resist-stripping sample (Fig. 2) is probably due to the pore sealing action of the –CF– based etch-byproduct. In the case of the 'with SiC cap', not only the –CF– based byproduct, but also etch-byproducts due to the SiC cap are formed (such as inorganic material sputter deposited from SiC cap). The byproducts of the SiC cap form a thicker and denser film enough to prevent penetration completely.

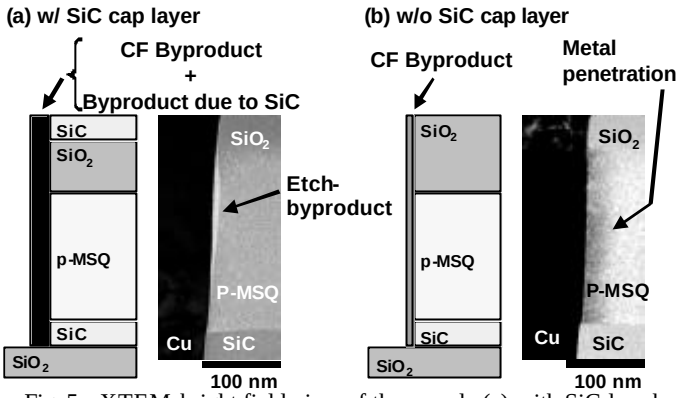

Fig. 5 XTEM bright field view of the sample (a) with SiC low-k cap and (b) without SiC low-k cap.

Two level Cu/p-MSQ single damascene interconnects were fabricated with ALD-TaN (1 nm) barrier metal and etch-byproduct pore sealing with the SiC low-k cap. Figure 6 shows the cumulative probability of the leakage current. Those of CVD pore-sealing method (CVD-SiC 15 nm at field area) are also shown in the figure for reference. Low leakage current for the etch-byproduct method, as low as the reference, was obtained. The via resistance of ALD was slightly lower than with the reference due to the thinner pore-seal thickness at the via. Excellent electrical characteristics were thus obtained by using etch-byproduct method.

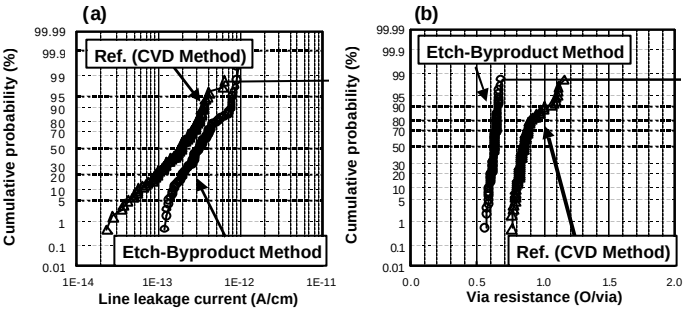

Fig. 6 Cumulative probability of (a) line leakage current of L/S = 0.16/0.16 μm and (b) via resistance of 50k chains with ϕ = 0.16 μm and L/S = 0.16/0.16 μm.

4. Conclusions

Cu and Ta penetration after Cu/ALD metallization onto porous MSQ was investigated. It was found that the thick and dense etch-byproduct due to the SiC low-k cap completely prevented penetration. Two level Cu/p-MSQ single damascene interconnects with ALD-TaN barrier metal and the etch-byproducts pore-sealing method showed excellent electrical characteristics.

Acknowledgements

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References

[1] T. Mourie et al, in Proc. of IITC 2003, p. 245 (2003).

[2] N. Ohtsuka et al, in Proc. of AMC 2003 (2003).