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Pentacene TFTs Fabricated by High-aspect Ratio Metal Shadow Mask

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1. Introduction

Among various organic semiconductors, pentacene continues to be an attractive material choice because of its high mobility on the order of 1 cm^2/Vsec for a variety of electronic applications, including information displays [1-3], electronic paper [4], and radio frequency identification (RFID) [5]. Even though pentacene thin film transistors (TFTs) can be implemented in one of two configurations, i.e., top contact and bottom contact [6], the best performances of pentacene TFTs in the literature [7,8] have always been demonstrated in the top contact configuration due to the inherently favorable conditions of pentacene growth compared with bottom contact mode [6]. However, the top contact mode is incompatible with the conventional photolithography for the definition of source and drain (S/D) electrodes on organic semiconductors due to their intolerance to the exposure of solvents and other liquids [9]. Therefore, metal shadow masks are generally used to define the top S/D contacts on organic materials because they can guarantee simple S/D definition process without damage of organic materials. But the S/D patterning process by the conventional metal shadow mask ($L_C \approx 20\sim70$ μm) [6], [9] has two major obstacles, which are high-resolution patterning [10] and mass manufacturability. While commercial products like OLED eliminate gradually the pessimistic prospect for the applications of a metal shadow mask to mass production [11], the high-resolution patterning using shadow masks can be a remaining barrier on highly integrated top-contact OTFTs [8].

To achieve top-contact OTFTs with a high areal density, several approaches including cold welding [12], high resolution rubber stamping [13] and special Si membrane masks ($L_C \approx 10$ μm) [14] have been reported in the literature, whereas each method has fundamental drawbacks of too much-complicated implementation [12], low-level manufacturability for large area applications [13], and easy brittleness [14].

In this work, we proposed and implemented metal shadow masks with a high aspect ratio (AR) larger than 20, based on a combination of anisotropic micro-electro-discharge machining (μ-EDM) [15] and isotropic electro chemical etching (ECE) [16] for the application of OTFTs scaled down to less than 5 μm. The high-aspect ratio (HR) metal shadow masks have inherent merits of structural robustness, simple S/D patterning process, and re-usage. In addition, a batch mode μ-EDM technique [17] can be fundamentally applicable to metals shadow masks of a high throughput and good uniformity for large area applications.

2. Experimental and Results

Figure 1 presents a schematic illustration of (a) μ-EDM [15] and (b) ECE [16], which were used to fabricate metal shadow masks with high AR larger than 20. As shown in Fig. 1(a), an AR for a metal shadow mask is defined as the thickness of a shadow mask (T_S) to the length of a bridge (L_C). In this experiment, μ-EDM system used the applied voltage of 100 V, a single RC pulse timing circuits with 500 pF and 1 kΩ, and a square copper electrode with one side length of 130 μm and structural height of 1500 μm fabricated by wire electrode discharge gliding (WEDG)[18]. The work pieces for shadow masks are 100 ± 5 μm thick stainless steel (304 SS) with the size of 1.5 cm × 1.5 cm. After serially machining

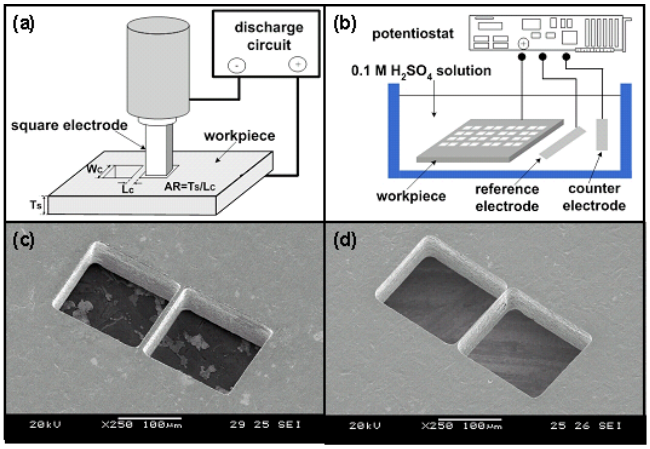
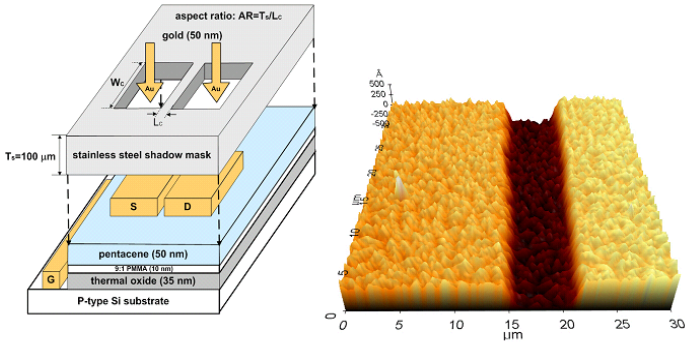


FIG 1. Schematic configurations for (a) micro-electro-discharge machining (μ-EDM) and (b) electro-chemical etching (ECE). The aspect ratio (AR) of an HR shadow mask denotes the ratio of the thickness of workpiece (T_S) to the length of a bridge (L_C). After μ-EDM processing up to the channel length of 10 μm, the work piece consecutively was electro chemically etched with an etch rate of 4.4 Å/sec in 0.1 mole H_2SO_4 solution (c) A SEM image for a stainless steel shadow mask right after μ-EDM process. After μ-EDM process, L_C is 10 μm with an aspect ratio of 10 (d) A SEM image for a metal shadow mask right after μ-EDM and ECE process. L_C is 3.5 μm with an aspect ratio of 28. The width of bridge (W_C) is 150 μm.

150 μm square contact holes using μ-EDM, the combinational process of ECE improves the AR of a metal shadow mask noticeably because the μ-EDM has a fundamental limit of the routinely machinable feature size ($L_C \approx 10$ μm) as shown in Fig. 1(c). Figure 1(b) shows that process conditions of ECE system are the applied voltage of 1.2 V and the 0.1 mole H_2SO_4 solution as electrolyte. Figure 1 (c) and (d) showed SEM images for a metal shadow mask after μ-EDM and ECE steps, respectively. To date, the length (L_C) and width (W_C) of the bridge can be routinely obtained as small as 5 ± 0.25 μm and 70 ± 1 μm, respectively.

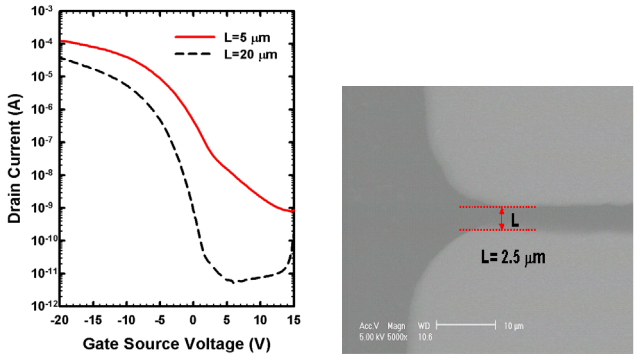
Figure 2(a) shows a schematic for the fabrication steps of pentacene TFTs. For a gate insulator, 35 nm thick thermal oxide was grown on a p-type wafer with the resistivity of 15 Ωcm. The thermal oxide was patterned by photolithography, and then etched by dilute HF solution for a gate electrode deposition. After cutting the patterned Si wafer to the size of 2 cm × 2 cm, each sample was spin-coated with a dilute PMMA solution to improve the ordering of pentacene due to the hydrophobic ending group methyl radical ($-CH_3$) [19]. The coated PMMA thickness was 10 nm as measured by ellipsometery. A 50 nm thick pentacene was thermally evaporated on the PMMA treated gate oxide at a rate of about 0.3 Å/sec. During the deposition, the substrate temperature maintained at the temperature of 90 °C in the pressure of 8×10^{-8} torr. The pentacene of about 98 % purity was used without purification in this experiment. Finally 50 nm of gold was e-beam evaporated on pentacene active layer through a 100 μm thick HR shadow mask to define S/D contacts as well as the gate contacts. The dimension of source and drain contacts have the channel length ranging from 20 μm to 5 μm at a fixed channel width of 150 μm.

Figure 2 (b) shows the AFM image of channel area for an OTFT with W_C=150 μm and L_C=5 μm. As shown in Fig. 2 (b), the



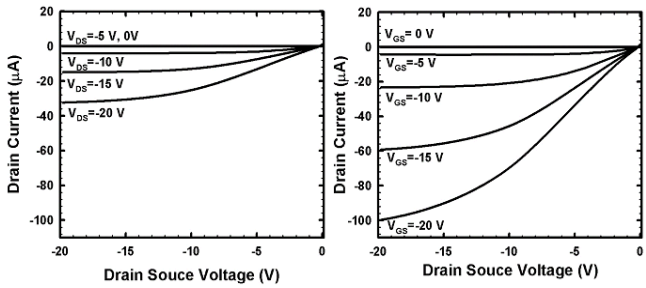
(a) (b)

FIG 2. (a) Schematic illustration of process steps for pentacene TFTs fabricated using an HR metal shadow mask. The length of a bridge (L_C) for metal shadow masks ranges from 20 μm to 5 μm with a fixed channel width of 150 μm (b) An AFM image for the defined channel area of OTFT with L_C=5 μm and W= 150 μm.



(a) (b)

FIG 3. (a) Transfer characteristics of pentacene TFTs with L_C=5 μm and L_C=20 μm in the saturation region (b) a SEM image for the locally abnormal parasitic OTFT with L_C=2.5 μm.



(a) (b)

Fig. 4. Output characteristics of pentacene TFTs with (a) L_C= 20 μm and (b) L_C= 5 μm for a fixed channel width of 150 μm.

defined source and drain contacts have a good straight channel.

Figure 3 (a) shows the transfer characteristics of OTFTs with a different L_C of 5 and 20 μm for a fixed W_C of 150 μm in the saturation region. For the device with L_C of 20 μm, electrical parameters are the threshold voltage (V_{TH}) of –1.3 V, subthreshold swing (SS) of 1.2 V/decade, current on-off ratio of 7.1×10^6, field effect mobility (μ_{eff}) of 0.421 ± 0.07 cm^2/Vsec at gate-source voltage (V_{GS}) of –10 V and drain-source voltage (V_{DS}) of –20 V. On the other hand, the device with L_C of 5 μm has V_{TH} of 3.3 V, SS of 1.2 V/decade, μ_{eff} of 0.498 ± 0.05 cm^2/Vsec at the same V_{GS} and V_{DS}. As the L_C of OTFT reduces from 20 μm to 5 μm, V_{TH} was shifted toward positive voltage from –1.3 V to 3.3 V. The current on-off ratio and SS was deteriorated from 7.1×10^6 to 1.6×10^5 and from 1.2 V/decade to 5.7 V/decade, respectively.

The result is thought to be attributed to the scaling-down effects of OTFTs, i.e. short channel effect [20], which V_{TH} increases from negative voltage to positive voltage as L_C decreases. In addition, the hump effects [21] of OTFTs fabricated by the HR shadow mask having L_C= 5 μm enhance the conspicuous change of V_{TH}, SS and current on-off ratio because the parasitic OTFT with L_C= 2.5 μm is turned on before the main OTFT with L_C= 5 μm as shown in Fig. 3 (b). Figure 3(b) shows that the L_C has locally abnormal channel of 2.5 μm in the OTFT due to the strong electric field around the corner of electrode during μ-EDM process.

Figure 4 shows the output characteristics of pentacene TFTs with L_C of (a) 5 μm and (b) 20 μm. For the OTFTs with L_C=5 μm and L_C=20 μm at V_{GS}=-10 V and V_{DS}=-20 V, the saturated drain current (I_{DSS}) was I_{DSS} =-24 μA and I_{DSS}=-4 μA, respectively. The measured saturation current ratio of (-24 μA)/(-4 μA) was obtained as 6. The significant improvement of current drivability was achieved from scaling down L_C from 20 μm to 5 μm at the same W_C of 150 μm. The result is meaningful because OTFTs of high current drivability consuming the same layout-area are highly demanded to achieve high-resolution flat panel displays based on OTFTs.

3. Conclusions

Metal shadow masks with a high aspect ratio (AR>20) using micro-EDM and ECE were proposed for high definition of S/D contacts (L ≤ 5 μm and W ≤ 150 μm) on organic semiconductors. The fabricated pentacene TFTs with the channel length of about 5 μm showed routinely mobility of 0.49 ± 0.025 cm^2/Vsec and current on-off ratio of 10^5. The HR metal shadow masks with AR larger than 20 can be used repeatedly for S/D electrodes deposition due to the structural robustness. The pentacene TFTs by HR shadow masks can meet the required OLED pixel resolution (≤ 100 × 100 μm^2) as well as high current drivability through the scaling-down of the width of OTFTs [11]. In addition, a batch mode μ-EDM can potentially solve a throughput and yield problem of HR metal shadow mask generation.

Acknowledgements

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