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Gate Depletion Effect Reduction and Flat-band Voltage Control in Poly-Si/$HfAlO_x$ MOSFETs with Nanometer TaN Dots at the Top Interface

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1. Introduction

The poly-Si gates have a serious problem of the depletion effect which significantly reduces advantages of using high-k dielectric as a gate insulator. Therefore, introducing metal gates for advanced CMOS is strongly required. We have proposed a new gate stack structure with nanometer size metal (TaN) dots at the poly-Si/SiO_2 interface to suppress the poly-Si depletion effect without the mobility degradation [1], in which the flat-band voltage, V_{FB}, can be tuned for nMOSFET as well as for pMOSFET.

This paper reports the usefulness of the TaN dots at the poly-Si/$HfAlO_x$ interface for controlling V_{FB} and reducing the depletion effect by adding a simple process step in the conventional poly-Si gate process. Furthermore, we also discuss TaN dot effect on the V_{FB} control based on the Fermi-level pinning (FLP) model [2].

2. Experimental

The MOSFET fabrication process flow is summarized in **Fig. 1**. After the conventional LOCOS isolation, 4nm-thick $HfAlO_x$ was deposited by the ALD process on the 1.5nm-thick SiO_2 interfacial layer. Various thicknesses of TaN dots were deposited on $HfAlO_x$ by using the ultra-low pressure CVD [3]. Then, 150nm-thick undoped amorphous Si was deposited on the TaN dots at 525ºC. After the gate patterning, P or BF_2 of $3x10^{15}$ cm^{-2} was implanted at 30keV or 35keV, respectively, followed by 200nm-thick SiO_2 deposition. The activation annealing was carried out at 950ºC in N_2 ambient for 20 sec.

3. Results and Discussion

Figure 2 shows cross-sectional TEM images and a schematic illustration of n^+ poly-Si/TaN/$HfAlO_X$/SiO_2/Si structure with three kinds of TaN thickness after the MOSFET fabrication. It is shown that the deposited TaN forms a dot structure whose diameter is smaller than 5nm in the case of 1.0 and 1.5nm thick TaN deposition, being similar to the case in SiO_2 [1]. Furthermore, it was observed that the density of TaN dots was increased with TaN thickness up to 2.5nm and then the TaN grains were connected to each other.

Figure 3 shows the high frequency C-V characteristics of nMOSFETs. It is clearly shown that the poly-Si gate depletion is well suppressed by introducing TaN dots. By using a TaN layer thicker than 0.5nm, the inversion capacitance recovers to above 95% of the accumulation capacitance. It is also shown in Fig. 3 that the V_{FB} of nMOSCAP with 10nm-thick TaN shifts from the case of the poly-Si gate to the positive direction by about 0.4 V. This suggests that the effective work function ($\Phi_{m,eff}$) on $HfAlO_x$ can be varied from the value of n^+ poly-Si toward a larger value of TaN.

Figure 4 shows the V_{FB} shifts for n and pMOSCAPs as a function of the TaN thickness. The V_{FB} shows a constant value up to 1.0nm thick for both n and pMOS. This indicates that FLP observed in the poly-Si/Hf-based high-k devices [2], still works for the TaN-dot inserted poly-Si/$HfAlO_x$ interface. However, it is found that V_{FB} values for n and pMOS shift toward a positive direction with increasing TaN thickness over 1nm by 0.4 and 0.2V, respectively. Therefore, it is clear that the TaN dot effect overcomes the FLP effect.

Figure 5 shows the $\Phi_{m,eff}$ values of poly-Si and TaN gates (10nm-thick) determined both on SiO_2 and on $HfAlO_x$. These $\Phi_{m,eff}$ values are obtained from extrapolation of the V_{FB} versus EOT plots [4]. It is observed that the $\Phi_{m,eff}$ values of both n^+ and p^+ poly-Si gate/$HfAlO_x$ shift toward midgap direction by FLP, while the $\Phi_{m,eff}$ of TaN gate on $HfAlO_x$ is closer to the case of SiO_2. The arrow in Fig. 5 indicates the change of the $\Phi_{m,eff}$ as the TaN thickness increases, as already shown in Fig. 4.

Figure 6 shows a model for the depinning mechanism at poly-Si/$HfAlO_x$ interface by inserting TaN dot. Increasing the TaN dots density on $HfAlO_x$ decreases the average number of Si-Hf bonds formed at the interface, which might relax the pinning effect. The further details are not understood yet, but a similar effect is also observed at $PtSi_x$/HfO_2 interface [4]. **Figure 7** shows electron and hole mobility characteristics of n and pMOSFETs with and without 1nm thick TaN dot at the poly-Si/$HfAlO_x$ interface. No additional mobility degradation for both n and pMOSFETs at high E_{eff} of 0.8MV/cm are observed in the case of introducing TaN dots at the interface, as compared with the case of conventional n^+ and p^+ poly-Si gates.

4. Conclusions

We have investigated the usefulness of TaN dots at the poly-Si/$HfAlO_x$ interface for reducing poly-Si depletion effect and V_{FB} control through relaxing FLP effect. The poly-Si depletion effect is effectively suppressed without the additional mobility degradation, by depositing TaN thicker than 0.5nm on $HfAlO_x$. In addition, V_{FB} can be changed by a TaN layer thicker than 1nm, where the FLP at poly-Si/$HfAlO_x$ interface starts to relax. This metal dot process is fully compatible with the conventional poly-Si gate process for advanced high-k CMOS.

Acknowledgements

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References

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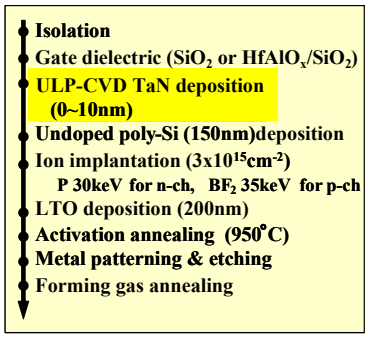

Fig. 1 MOSFET fabrication process flow for a new gate structure with TaN dots on $HfAlO_x$. It is fully compatible with the conventional poly-Si gate process.

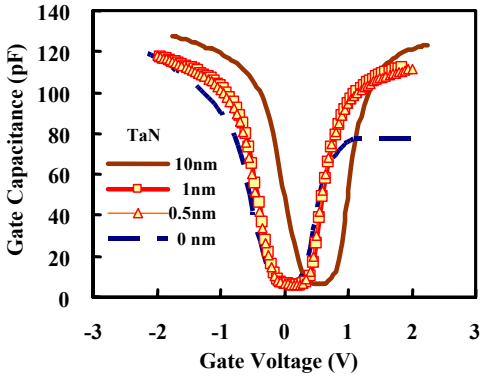

Fig. 3 High frequency C-V curves measured for nMOSFETs (L/W=100μm/100μm) from accumulation to inversion. It is clearly shown that the poly-Si gate depletion is well suppressed by introduced TaN dots. The inversion capacitance shows 95% of the accumulation one even in case of 0.5nm thick TaN dot.

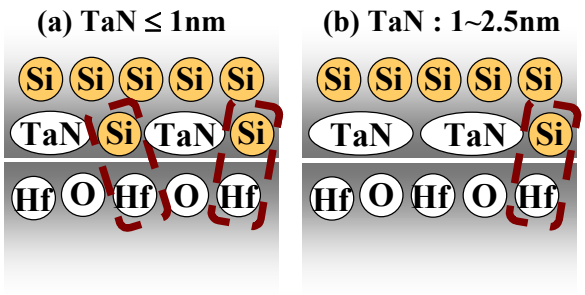

Fig. 6 A possible model of depinning mechanism at poly-Si/$HfAlO_x$ interface by inserting TaN dots. Increasing density of TaN dots on $HfAlO_x$ results in the decrease of Si-Hf bonds at the interface, which causes relaxation of the pinning effect.

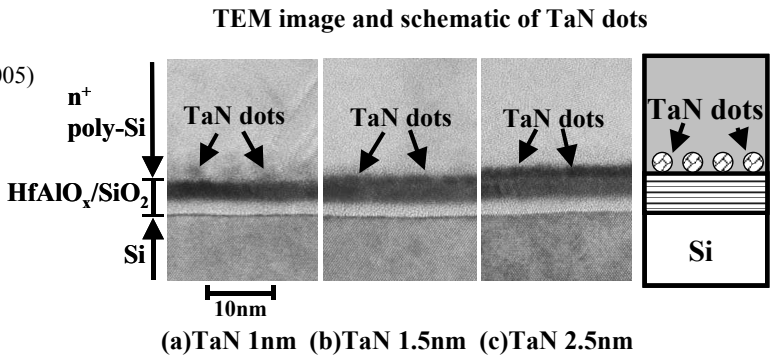

Fig. 2 Cross-sectional TEM images and schematic illustration of the n^+ poly-Si gate stack structure including TaN dots. TaN dots of 1~2.5nm thickness are deposited on $HfAlO_x$ films. TaN dots with less than 5nm diameter at the n^+ poly-Si/$HfAlO_x$ interface are observed in (a) and (b), while grains connect each other in (c).

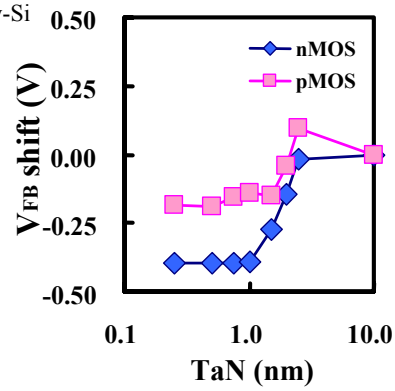

Fig. 4 V_{FB} shifts of poly-Si/TaN/$HfAlO_x$ n and pMOSCAPs as a function of the TaN thickness. The V_{FB} values of both MOSCAPs show a constant value up to 1nm because of FLP at poly-Si/$HfAlO_x$. In the range of 1-2.5nm thickness, the V_{FB} shifts toward the positive value because TaN dot effect overcomes the FLP effect.

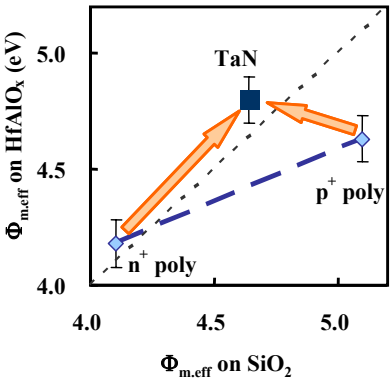

Fig. 5 Relationship between $\Phi_{m,eff}$ values of poly-Si and TaN gates on SiO_2 and $HfAlO_x$. TaN thickness is 10nm. It is observed that the $\Phi_{m,eff}$ of poly-Si gate is strongly affected by FLP on $HfAlO_x$, while the $\Phi_{m,eff}$ of TaN gate is little affected.

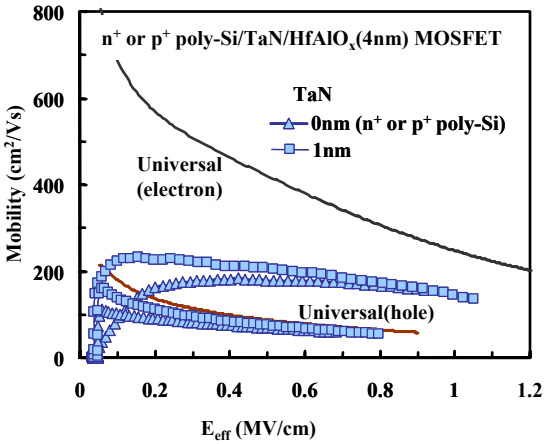

Fig. 7 The inversion layer mobility characteristics of poly-Si/TaN gate HfAlOx n and pMOSFETs. No additional mobility degradation for n and pMOSFETs are observed for the case of TaN dot gates, in comparison with simple poly-Si gate devices.