Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 8-9

A-1-1 (Invited)

Challenges for PMOS Metal Gate Electrodes and Solutions for Low Power Applications

J.K. Schaeffer[1], W.J. Taylor, S.B. Samavedam, D.C. Gilmer, D.H. Triyoso, R.I. Hegde, S. Kalpat, C. Capasso, M. Sadd, M. Stoker, A. Haggag, D. Roan, B.E. White Jr.

[1]Silicon Technology Solutions, Freescale Semiconductor,
2070 Route 52, Hopewell Junction, NY 12533, MD: IBM-EFK, NY22
Phone: 845-892-1733, E-mail: jamie.schaeffer@freescale.com

1. Introduction

One of the more fundamental stumbling blocks in the implementation of high-k / metal gate devices has been the inability to achive low pFET threshold voltages on silicon in a gate first integration. This problem has mostly been ascribed to Fermi level pinning at the metal-dielectric interface, but a new methodology for extracting effective work-function (Φ_{eff}) indicates other mechanisms might also play a significant role. Studying the V_{fb}-EOT characteristics of wafers with fixed $Hf_xZr_{1-x}O_2$ thickness/variable SiO_2 thickness/Silicon (cake oxide), a problem referred to as V_{fb} (or V_t) vs. EOT roll-off is observed. This talk will review the latest experiments that provide insights into the origin of this problem.[1] Although the pFET problem remains a mystery and its origins are of academic interest, new solutions are being engineered to circumvent this problem and enable the use of high-k/ metal gate devices for low power applications.

2. P-Channel Threshold Voltage

Experiment Details

To quantify V_{fb} roll-off cake oxides are created with two thick tiers with sufficiently thick SiO_2 where roll-off has not yet begun to occur and an outer-tier etched all the way down to Si. After the tier formation a wet clean is performed to re-grow a chemical oxide on the outer-tier before depositing ALD $Hf_xZr_{1-x}O_2$. ΔV_{fb} roll-off is defined by taking the average V_{fb} from the outer-tier and then subtracting from that the expected V_{fb} obtained by extrapolating the V_{fb}-EOT trend-line from the outer two tiers to the average EOT of the thin-tier, such that ΔV_{fb} roll-off = actual V_{fb} – expected V_{fb} (fig. 1).

Role of Processing Temperature

The role of processing temperature on V_{fb} roll-off was evaluated using $Si/SiO_2/Hf_xZr_{1-x}O_2/Mo_2N/TiN/W$ metal-oxide-semiconductor capacitors. A plot of V_t vs. EOT for the samples with 500°C S/D activation and with the 1000°C S/D activation indicates that the roll-off can be eliminated by removing the 1000°C anneal (fig. 2). The V_{fb} (V_t) roll-off is plotted versus temperature for all samples indicating that V_{fb} roll-off increases in magnitude with processing temperature (fig. 2 inset).

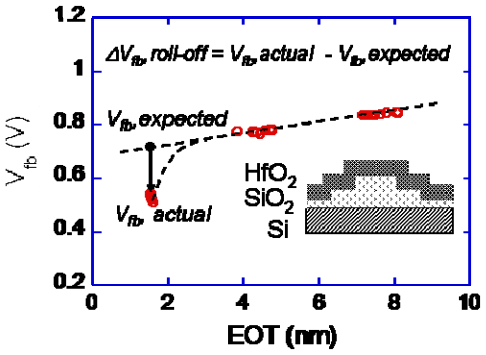

Fig. 1 ΔVfb roll-off behavior and picture of cake oxide formation.

Impact of Work Function and Substrate Doping

V_{fb} roll-off has been studied in detail with TaC (4.3eV), TiN (4.5eV), and Mo_2N (4.9eV) electrodes on both p-type (NMOS) and n-type (PMOS) substrates. Plotting the V_{fb} roll-off as a function of the HfO_2 physical thickness indicates that the roll-off is larger in magnitude and more negative for the high work-function Mo_2N gated devices than for TaC and TiN gated devices (fig. 3). Along with a strong work-function dependence this experiment also indicates that V_{fb} roll-off has a small substrate dependence. TaC, TiN, and Mo_2N gated devices all show that the V_{fb}-EOT roll-off is approximately 100mV more negative on p-type (NMOS) than on n-type (PMOS) substrates.

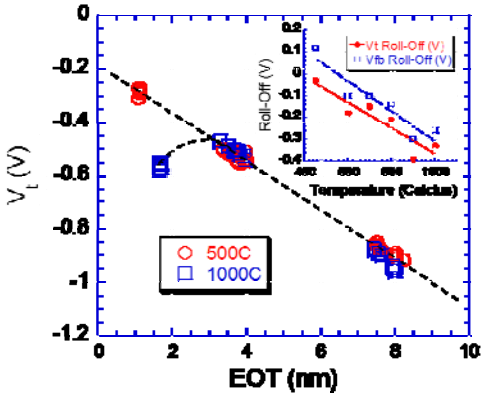

Fig. 2 Vt-EOT comparison for 500°C & 1000°C anneal and magnitude of the ΔVfb roll-off 500°C-1000°C (inset).

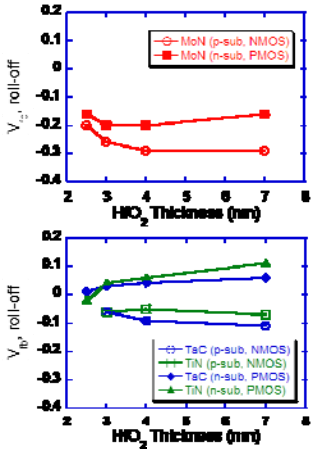

Fig. 3 Magnitude of ΔVfb roll-off (V) for Mo_2N (top) and TiN, TaC (bottom) for different HfO_2 thickness

Proximity of High-k to Substrate

To show that the V_{fb} roll-off effect is related to the proximity of the high-k film to the substrate an experiment where just 1 cycle of ALD HfO_2 was deposited on the cake oxide and then capped with thick SiO_2 prior to the electrode deposition was performed. When compared to a control sample without the 1cy of HfO_2, the experiment suggests that even with the insertion of 60Å of SiO_2 between the electrode and HfO_2 there is still V_{fb} roll-off (fig. 4). This indicates that it is proximity of the HfO_2 to the substrate and not a charge exchange between the HfO_2 and the electrode responsible for the elevated pFET Vts.

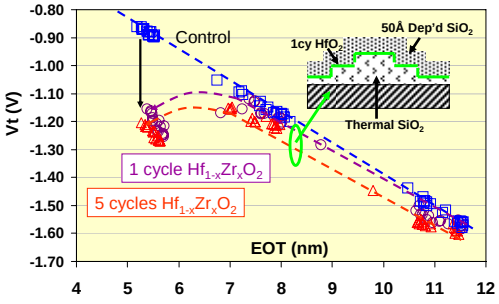

Fig. 4 Vt-EOT behavior for cake oxide/60Å SiO_2 versus cake oxide/1-5cy HfO_2/60Å SiO_2.

Impact of Dielectric Material

V_{fb} roll-off was compared on HfO_2 and Al_2O_3 dielectrics with TaC, TiN, and Mo_2N electrodes. The result indicates that the V_{fb} roll-off is ~100mV more negative on Al_2O_3 for each electrode compared to what is shown on HfO_2 in figure 3.

3. Solutions for Low Power Applications

Experiment Details

Creative engineering solutions are being proposed to solve the fundamental pFET threshold voltage problem. It was discussed earlier that low temperature processing, such as in a replacement gate integration, is one possible method to achieve low pFET threshold voltages. Another solution that has been recently presented is to use SiGe-based channels [2] where the valence band off-set between silicon and germanium is more favorable for low pFET threshold voltages. Finally, another solution that was recently discussed is one that uses a single metal gate electrode with a high performing nFET coupled with a counter-doped pFET device. [3]

TaC, with a work function of ~4.3eV, ideal for low power devices according to simulations, can be used for both n/p devices. With a T_{inv} of 16Å, the TaC/$HfZrO_4$-based nFET produces a 1.0V (1.2V) $I_{d,sat}$ of 850μA/μm at I_{off} = 1nA/μm (1550μA/μm at I_{off} = 100nA/um). By using the same gate electrode and counter-doping the pFET, Tinv of 18Å and Id_{sat} of 325μA/um at 1nA/μm Ioff is achieved. (fig. 5)

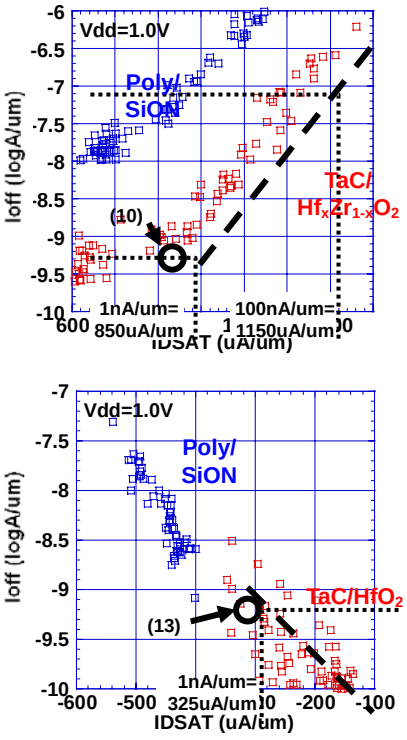

Fig. 5 Ion-Ioff plots for TaC nFET and TaC buried channel pFET

4. Conclusions

Clear evidence has been provided indicating that the V_{fb} roll-off (1.) is a result of placing high-k in close proximity to the substrate, (2.) is a result of exposing the high-k to elevated processing temperatures, (3.) depends on the substrate and metal Fermi levels, and (4.) is not unique to Hf-based high-k gate dielectrics. In spite of these fundamental issues solutions are being engineered to circumvent this problem. One such solution is to use a counter-doped channel with an nFET-like (TaC) metal gate electrode to meet the criteria for low power 45nm technologies.

References

[1] J. Schaeffer, submitted to J. Appl. Phys. 2007
[2] R. Harris, et al., VLSI, 2007
[3] W.J. Taylor, et al., IEDM 2006