Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 36-37

B-1-4

Pt-germanide Formed by Laser Annealing and Its Application for Schottky Source/Drain MOSFET Integrated with TaN/CVD-HfO_2/Ge Gate Stack

Rui Li[1], S. J. Lee[1], D. Z. Chi[2], M. H. Hong[3] and D. -L. Kwong[4]

[1]Silicon Nano Device Lab, Department of ECE, National University of Singapore, 10 Kent Ridge Crescent, Singapore, 119260 Email: elelsj@nus.edu.sg Phone: (65) 65166140 Fax: (65) 65161589 [2]Institute of Materials Research and Engineering, Singapore, 117602 [3]Laser Microprocessing Lab, Department of Electrical and Computer Engineering, National University of Singapore, 10 Kent Ridge Crescent, Singapore, 119260 [4] Institute of Microelectronics, Singapore, 117685

Abstract:

For the first time, the comprehensive study on the formation and characteristics of Pt-germanides formed by laser annealing is presented. Excellent morphology and sharp interface with Ge are achieved by laser annealed Pt-germanides, along with extremely low hole barrier height of 0.08eV, showing that Pt-germanide by laser annealing is promising approach for high-performance conventional self-aligned CMOSFET application. Pt-germanides Schottky S/D transistor by laser annealing integrated with CVD-HfO_2/TaN gate stack is also demonstrated.

I. Introduction:

Ge-channel MOSFETs have been considered as one of the most promising solutions for future high performance CMOS technology due to the higher carrier mobility of Ge. Although Ge MOSFETs with enhanced mobility integrated with high-k dielectric and metal gate have successfully been demonstrated by using surface passivation techniques [1-3], limited thermal stability of Ge/high-k/metal gate stack, dopant solid solubility limits, difficulties in formation of ultra-shallow source/drain junction as well as its large resistance, have been considered as bottleneck for future developing of Ge MOSFETs. Schottky S/D structure is an attractive alternative to conventional-doped S/D to overcome these challenges by providing advantages of low formation temperature, atomically sharp junction, low resistivity and a simpler implantless fabrication process. In previous works we have successfully demonstrated metal-germanides Schottky S/D MOSFETs with improved performance compared to conventional-doped S/D, and Pt-germanide has been shown to be one of the most promising candidates for p-MOSFET [4-6]. However, all previous studies were carried out by subjecting the whole device wafer to an elevated temperature using RTA. As an alternative, a laser annealing process could offer following advantages: (1) Local selective heating of specific regions and reduced thermal budget. (2) Tailored germanide profile due to the suppressed metal and Ge diffusion. (3) Improved interface between germanide/Ge due to the suppressed diffusion of impurities in short process. (4) Reduced process cost and increased process flexibility. In this work, we report the investigation of Pt-germanides formation by laser annealing process and demonstrate the feasibility of laser annealed Schottky S/D p-MOSFETs integrated with HfO_2/TaN gate stack.

II. Experiments:

In order to study the properties of Pt-germanide and its process optimization, Pt was deposited onto (100) N-type Ge wafers after removal of native oxide on the wafer surface by dipping into DHF. A KrF excimer laser with a wavelength of 248nm was used to irradiate the sample to form germanides with laser fluence ranging from 0.10~0.22J/cm^2 for 1 to 10 pulses. The laser pulses were produced at a repetition frequency of 1 Hz and pulse duration of 23ns. For the fabrication of Pt-germanide Schottky S/D MOSFETs, Ge substrate received plasma PH_3 treatment to improve interface quality [1], followed by MOCVD HfO_2 deposition and reactive sputtering of TaN to form the gate electrode. After spacer formation and S/D Pt deposition, samples were irritated at 0.14J/cm^2 for 1 pulse. A schematic sketch of the laser annealing experimental setup is shown in Fig. 1. Finally, unreacted Pt was removed by dry etching.

III. Results and discussion:

Fig. 2 shows SEM images of Pt/Ge samples after laser annealing. Up to the fluence of 0.18J/cm^2 for 1 pulse and 10 pulses, smooth morphology and uniform Pt-germanide films without significant agglomeration were observed, as shown in Fig. 2 (a), (b) and (c), which are similar with the morphology of Pt- germanide formed by an optimized RTA at 400°C (Fig.2 (f)) [4]. However, an apparent agglomeration for 0.20J/cm^2 and increased agglomeration for 0.22 J/cm^2 were observed in Fig. 2 (d) and (e). XRD results are shown in Fig. 3. No obvious reaction happens at 0.10J/cm^2 for 1 pulse in Fig. 3(a), however, Pt_3Ge_2 peaks are detected as pulse number increases. In Fig. 3(b), when samples were annealed at 0.14J/cm^2 from 1 to 10 pulses, intensities of Pt_3Ge_2 phases decrease and finally most were replaced by $PtGe_2$ phase. Co-existence of 2 phases of Pt-rich germanide and $PtGe_2$ can be attributed to the rapid melting and re-solid process, by which the inter-diffusion of metal and Ge and redistribution of metal atoms are greatly suppressed during each laser pulse irritation, resulting in a film with varying Pt-Ge concentration starting with Ge rich at the Pt-Ge interface to Pt rich at the surface. The similar trend was also observed for samples annealed at other fluence. Unlike the Pt-germanides formed by RTA, by which germanide phase formation is determined by temperature [6], same phase can be obtained at various laser fluence at specific pulse number, as shown in Fig. 3(c). TEM pictures in Fig. 4 show that uniform Pt- germanide films are formed with sharp interface with the Ge substrates. Epitaxial growth of Pt germanides on Ge substrate is also observed in high-resolution TEM in Fig. 4(b).

A laser irritation at 0.14J/cm^2 for 1 pulse was applied to form S/D of Pt-germanide Schottky S/D MOSFETs, in order to minimize the damage on gate stack. I-V characteristics measured from Schottky diode at S/D region is shown in Fig. 5. By fitting the forward current using traditional thermal emission model [7], an electron barrier height, $q\varphi_{be}$ of 0.58eV was obtained, meaning a hole barrier height of 0.08eV, which is quite close to the data previously reported in [6]. C-V and I-V characteristics of TaN/HfO_2/Ge gate stack in Fig. 6, show V_{FB} of −1 V and low leakage of 10^{-4}A/cm^2 at $|Vg-V_{FB}|$= 1V. Fig. 7 shows a well-behaved I_D-V_D output characteristics of laser annealed Pt-germanide Schottky S/D Ge p-MOSFET with channel width/length = 400/10μm. However, a poor sub-threshold characteristics shown in Fig. 8 indicates that further process optimization, including capping layer to protect gate stack during laser annealing, is required.

IV. Conclusions:

Pt-germanide formation by laser thermal annealing is systematically studied for the first time. Pt-germanide with good morphology, sharp interface with Ge, and low hole barrier height of 0.08eV is obtained by laser annealing and the feasibility making Schottky S/D MOSFET integrated with HfO_2/TaN gate stack is demonstrated.

[1] S. J. Whang, et al., IEDM 2004, [2] C. O. Chui, et al., IEDM 2003, [3] N. Wu, et al., EDL 2004 [4] R, Li, et al., EDL 2006, [5] F. Gao, et al., VLSI 2006,[6] H. B. Yao, et al., APL, 2006. [7] S. Y. Zhu, et al., EDL 2005.

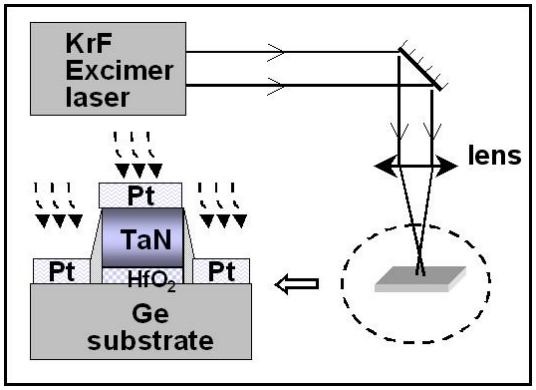

Fig. 1. A schematic sketch of the laser annealing experimental setup and transistor structure.

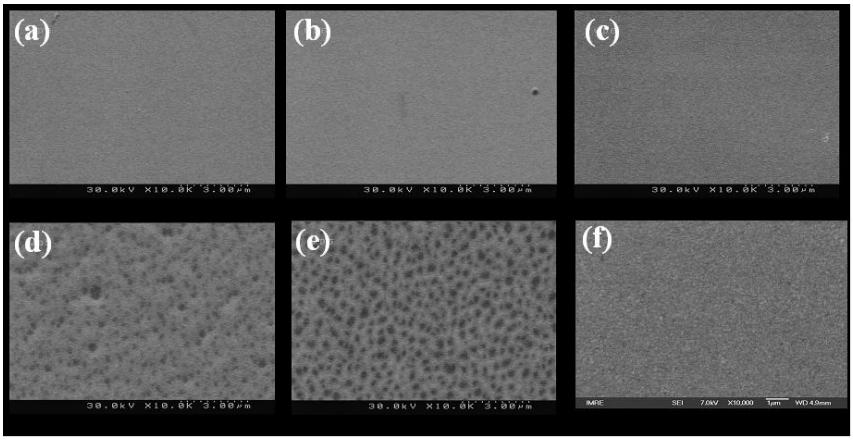

Fig. 2. SEM images of Pt/Ge by laser annealing at (a) 0.10J/cm^2 for 1pulse, (b) 0.18J/cm^2 for 1pulse, (c) 0.18J/cm^2 for 10pulses, (d) 0.20J/cm^2 for 1pulse, (e) 0.22J/cm^2 for 1pulse and by RTA at (f) 400° C.

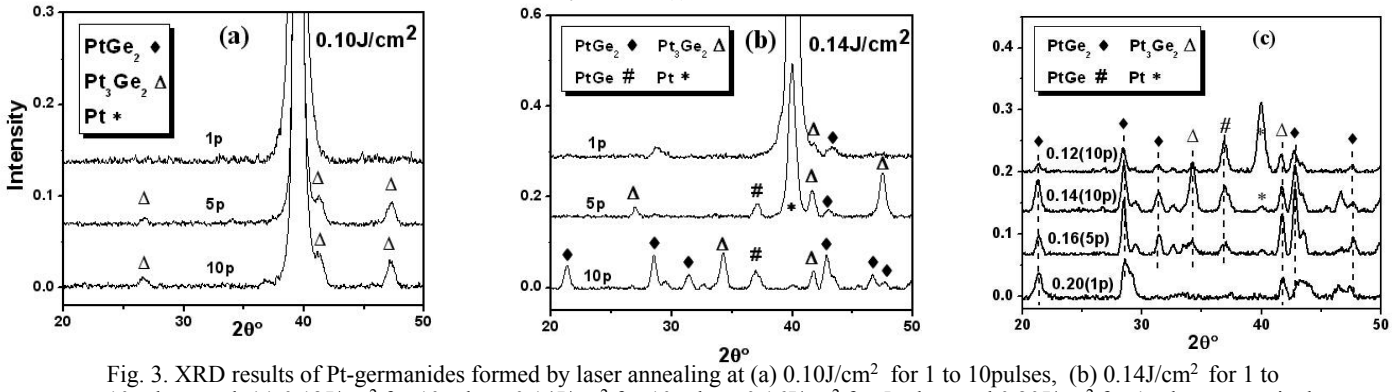

Fig. 3. XRD results of Pt-germanides formed by laser annealing at (a) 0.10J/cm^2 for 1 to 10pulses, (b) 0.14J/cm^2 for 1 to 10pulses ,and (c) 0.12J/cm^2 for 10pulses, 0.14J/cm^2 for 10pulses, 0.16J/cm^2 for 5pulses and 0.20J/cm^2 for 1pulse, respectively.

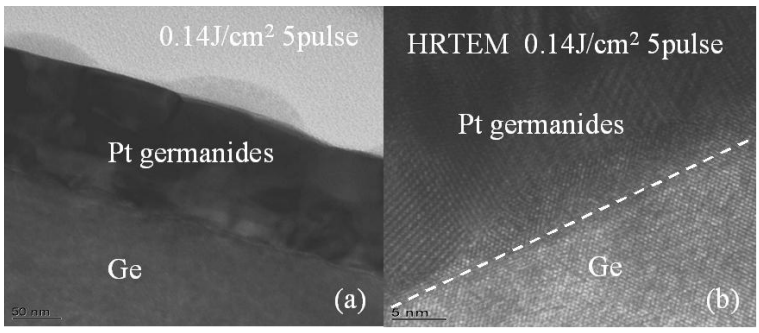

Fig. 4. (a) TEM and (b) HRTEM pictures of Pt-germanides formed by laser annealing at 0.14J/cm^2 for 5 pulses.

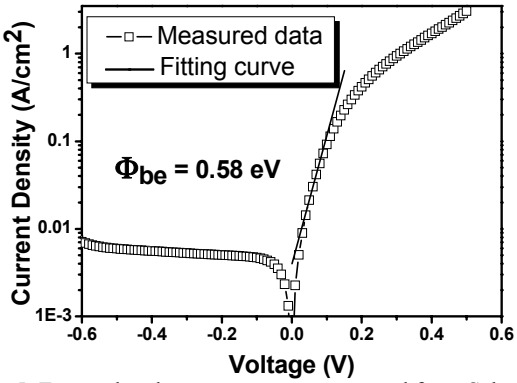

Fig. 5. Forward and reverse current measured from Schottky diode at S/D region of Pt-germanide Schottky S/D MOSFET by laser annealing at 0.14J/cm^2 for 1pulse.

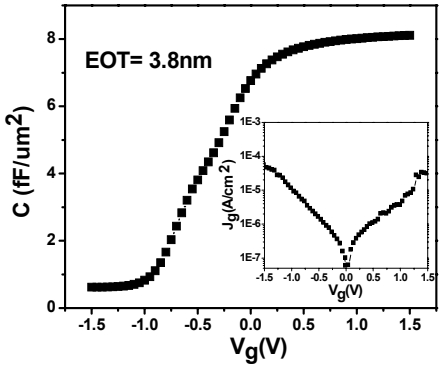

Fig. 6. C-V and I-V characteristics of TaN/HfO$_2$/Ge gate stack of Pt-germanide Schottky S/D MOSFET by laser annealing.

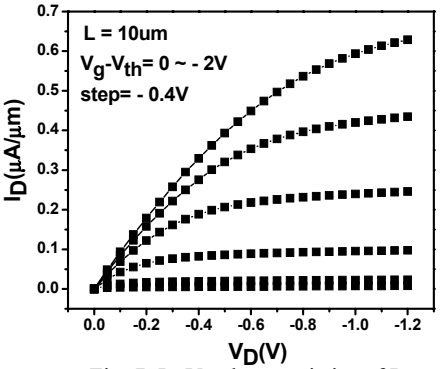

Fig. 7. I_D-V_D characteristics of Pt-germanide Schottky S/D MOSFET by laser annealing.

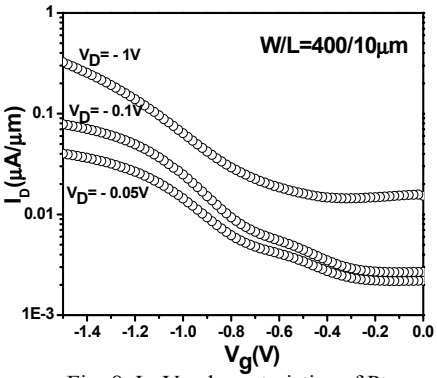

Fig. 8. I_D-V_G characteristics of Pt-germanide Schottky S/D MOSFET by laser annealing.