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Additive Process Induced Strain (APIS) Technology for L_g = 30nm Band-Edge High-k/Metal Gate nMOSFET

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Abstract

We report a novel method of performance enhancement (21%) in drive current via **additive process induced strain technology** that incorporates both a stressor contact etch stop layer (sCESL) and a stressor spacer in **short channel (L_g=30nm) band-edge (V_t = 0.3V @ EOT = 1.1nm) high-k/metal gate nMOSFETs**. This demonstration also illustrates compatibility and effectiveness of strain engineering with short channel high-k/metal gate band edge devices. A blanket tensile film results in a compressive spacer that translates tensile stress in the local channel area improving nMOS drive current.

Introduction:

Aggressive scaling of *C*omplementary *M*etal *O*xide *S*emiconductor *F*ield *E*ffect *T*ransistor (CMOSFET) technology requires a high drive current to increase circuit speed. Mobility enhancement by substrate engineering or process induced strain gives high source injection velocity into the quasi-ballistic transport channel [1, 2]. From the 65nm node, introduction of SiGe and/or stressor nitride in *C*ontact *E*tch *S*top *L*iner (CESL) for pMOS and nMOS performance enhancement, respectively was established as a mature technology [3, 4]. However, continued scaling of the device structure and introduction of high-k/metal gate devices from 45nm node requires development of new scaled down stressor and/or transforming passive components of the MOSFET devices (example: spacer, ILD, etc.) into stressor layers. To this end, we report using stressor Si_3N_4 as spacer film along with conventional sCESL for performance enhancement in short L_g band-edge high-k/metal gate nMOSFETs.

Experiment:

The process flow is detailed in table 1 and the fabricated 32nm nMOSFET image is shown in Fig. 1. Hf-La based work function engineering enables band edge nMOSFET (Fig. 2) achievement of low EOT (Fig. 3). We compared a control wafer with Si_3N_4 (0.05GPa) spacer and CESL, a split of a tensile CESL (+1.5GPa), a split of a tensile stressor with a split of tensile sCESL plus tensile spacer. Stress of the spacer films are obtained from global stress measurement.

Results:

Output characteristics of the fabricated device (Fig. 4) show clear trend of increased output current for additive process induced strain technology. Specifically, I_{on}-I_{off} for L_g = 60nm gate devices also show around 21% increment in I_{on} at I_{off} = 100nA/μm (Fig. 5). Transconductance is also increased by APIS (Fig. 6). The drive current enhancement plot for various gate lengths (Fig. 7) shows a clear trend of more performance gain for short channel devices. Given that the spacer width is uniform for all channel lengths, it is not surprising that the stressed channel volume fraction and therefore drive current enhancement increases for the shortest L_g devices. The percentage performance enhancement calculated from I_d-L_g plot shows 21% increase in I_{on} values between control and APIS for nMOSFET at L_g=100nm. Comparing with uniaxial longitudinal tensile stress plot for Si (100) nMOSFET shows that ~600MPa of uniaxial stress can be generated by the stressor spacers [5]. To differentiate whether $R_{S/D}$ reduction is contributing in the drive current enhancement, we measured the $R_{S/D}$ for nMOSFETs with and without APIS and found there is no difference. Therefore, we can exclude $R_{S/D}$ reduction contribution for enhanced drive current in the stressor spacer devices. The performance gain with stressor spacer may originate from the enhanced carrier mobility (Fig. 8) due to the local stretching of the channel region (Fig. 9a). Another hypothesis is because of compressively stressed spacer for nMOSFET device, during the S/D activation anneal poly-Si gate cap evolves tensile stress in the vertical direction which ultimately results in lateral tension in the channel region (Fig. 9b). To hold both of these hypotheses, it is expected that the channel length will play an important role for effective transformation of the spacer induced strain in to the channel. Fig. 3 clearly shows that the drive current is enhanced with short L_g devices. Therefore, it may be both of the effects playing important role to performance enhancement in APIS. Finally, the *P*ositive *B*ias *T*emperature *I*nstability (PBTI) results for various overdrive conditions clearly show no significant different in V_t shift due to the APIS technology (Fig. 10). It is understandable that substrate-strain results in biaxial strain to channel and enhances carrier mobility. However, cost, scalability, complexity such as low defect eSiGe buffers, low thermal budget, and integration are challenging. Moreover, the hole mobility of the Si channel at high fields is not improved significantly except at the Ge or dual channel because the energy separation between light and heavy hole bands is not enough due to the quantization effect. In contrast, uniaxial strain offers similar electron mobility enhancement compared with biaxial strain, while the hole mobility improvement is more significant at high field. Therefore, additive process induced strain technology like the demonstrated stressor spacer plus sCESL induced performance enhancement offers more opportunity. Also, spacer is an integral part of a CMOSFET and for short channel devices it is in more close proximity of the channel. Thus, APIS provides more benefit.

Conclusion:

We demonstrate that stressor spacer (like stressor Si_3N_4) can be used to transfer stress into the channel for short channel devices in band-edge high-k/metal gate MOSFETs. This is an effective way to introduce spacer stress induced device performance enhancement without interrupting other device critical factors. As spacer is an integral passive component of a device, therefore, application of stressor spacer is a unique method for new sort of process induced strain engineering. At the same time, this new strain engineering capability additively correlates with conventional sCESL, thus makes *APIS a useful and unique technology for short channel high-k/metal gate band edge devices*.

References:

[1] M. Lundstrom, IEDM Tech. Dig., 2003, pp. 789–792; [2] C. Jungemann et. al., IEDM Tech. Dig., 2003, pp. 191–194; [3] M. Fischetti et. al., J. of App. Phy. 80(4), p.2234-2252 (1996); [4] F. Andrieu, IEEE Elect. Dev. Let. 26(10), p.755-757 (2005); [5] S. Suthram et. al., IEEE Elect. Dev. Let., 28 (1), p.58-61 (2007).

Table 1: nMOSFET Flow

- Shallow Trench Isolation (STI)
- Well formation
- Hf + La based dielectric formation
- MeN_x metal + poly –Si deposition
- Gate Etch
- LDD/Halo implantation
- Spacer (APIS 1)
- S/D formation
- Spike anneal at 1000C
- $CoSi_2$
- Contact (APIS 2)
- Al based Metallization
- FGA

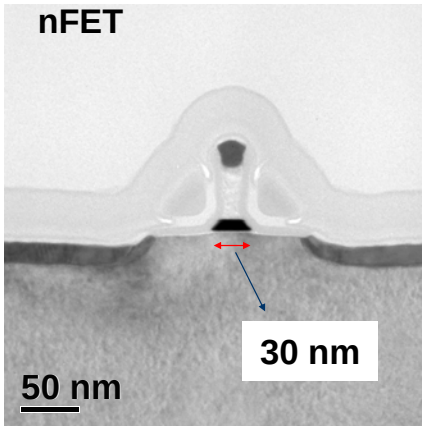

Fig. 1: Transmission electron microscopy (TEM) of nMOSFET

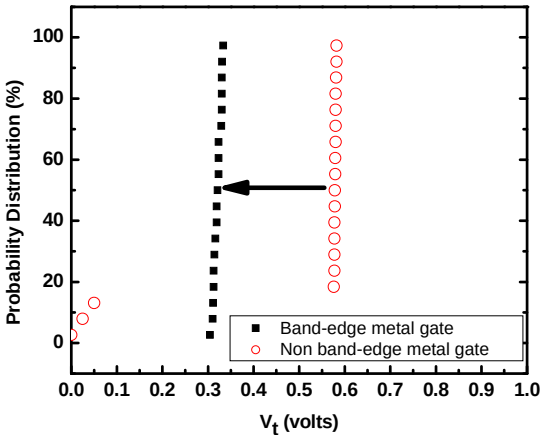

Fig. 2: Hf-La based W_f engineering for threshold voltage (V_t) tuning to achieve band-edge nMOSFET

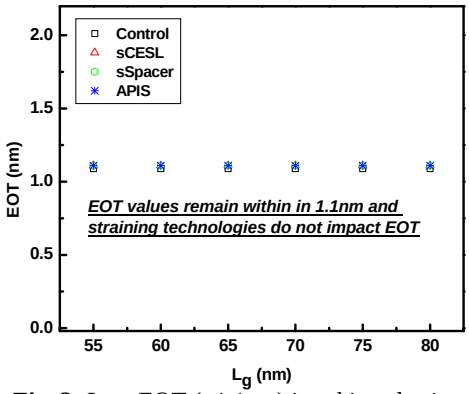

Fig. 3: Low EOT (~1.1nm) is achieved using band edge nMOSFET, promising for HP device

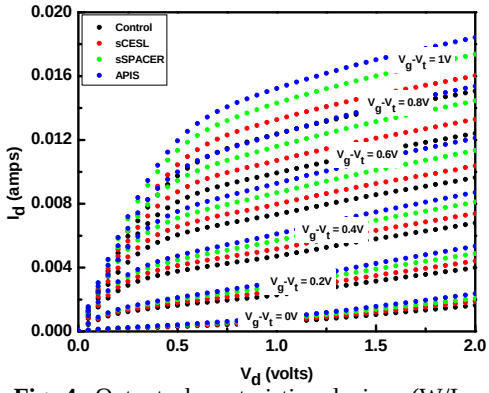

Fig. 4: Output characteristics devices (W/L_g = 10µm/100nm) show that APIS devices have clear performance enhancement.

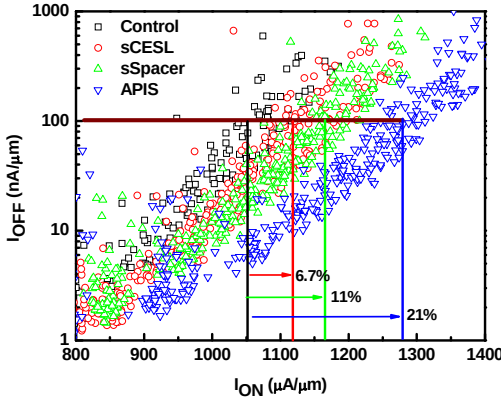

Fig. 5: I_{on}-I_{off} characteristics (W/L_g = 10µm/60nm) show around ~20% improvement for I_{off} = 100nA/µm. V_{dd} = 1V.

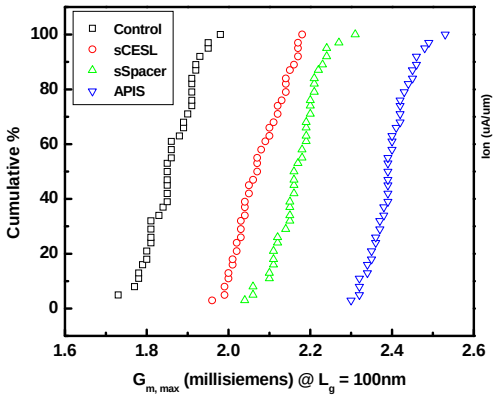

Fig. 6: Transconductance is improved for nMOS in the APIS devices.

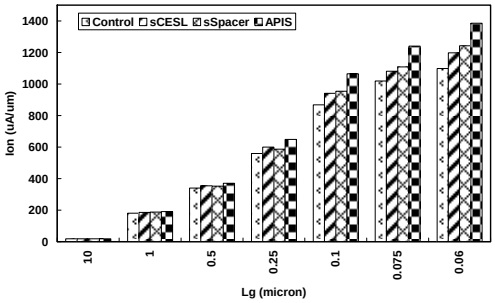

Fig. 7: Drive current enhancement with various L_g for nMOSFETs show that the enhancement is observed in short channel devices. This indicates stressor spacer induced effective stress transfer mechanism in short channel devices.

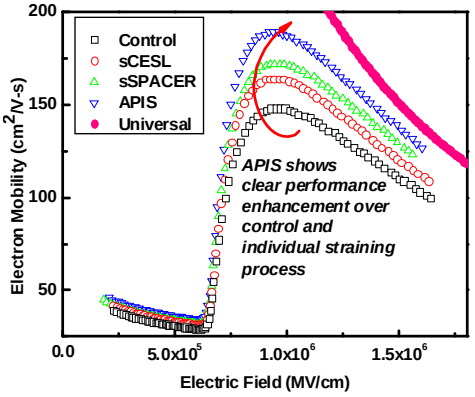

Fig. 8: Electron mobility for L_g = 80nm devices is significantly improved for nMOS with APIS.

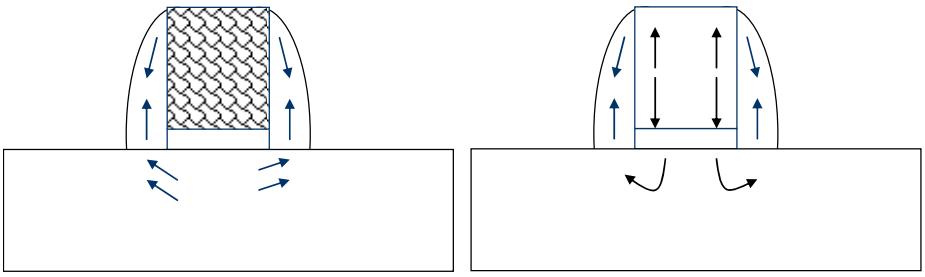

Fig. 9: There are two hypotheses under consideration: (a) due to tensile Si3N4 as spacer film, spacer is eventually compressive, therefore introducing a local tensile stretching of the channel to have nMOS performance enhancement; (b) compressive spacer can transfer stress during the activation anneal to the poly silicon gate capping where it will be tensile in vertical direction. This tensile stress may induce a lateral tension in the channel area.

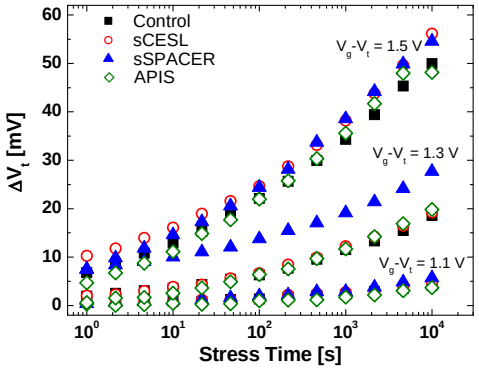

Fig. 10: PBTI verification shows APIS technology does not degrade device reliability.