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Evaluation of Electron and Hole Mobility at Identical MOS Interfaces by using Metal Source/Drain GOI MOSFETs

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1. Introduction

Recently, Ge has attracted much attention as a new material used for MOSFETs channels because of the scaling limit of Si CMOS technology. The Ge-channel MOSFETs are expected to improve the current drive, because of the higher carrier mobility than Si (2-3x for electron and 4x for hole). However, it has been pointed out that n-channel Ge MOSFETs exhibit the low electron mobility and the poor current drive, while high current drive has been achieved in p-channel Ge MOSFETs [1-3]. This low current drive in Ge n-MOSFETs has been attributed to higher interface state density near the conduction band edge [4] and the parasitic resistance of n^+/p source/drain (S/D) junctions [5]. However, the mechanism is still not clear.

In this study, we evaluate the electron and hole mobility only in the channels by eliminating the influence of parasitic resistance in S/D junctions, which is supposed to be one of the main causes of current drive degradation, in order to understand the difference of the current drive between Ge n- and p-MOSFETs. In particular, we successfully present the experimental results of the electron and hole mobility extracting from an identical metal S/D GOI MOSFET, for the first time, for the direct comparison between n- and p-MOSFETs.

2. Experiments

Metal S/D GOI MOSFETs [6, 7] with back gate control were used for mobility measurement in this study. The device structure is shown in Fig. 1. The GOI layers were fabricated by the Ge condensation method [8]. PtGe was used as the S/D metals. We measured the mobility at the interface between the buried oxide (BOX) layer and GOI layer. Here, the back gate structure is quite effective in avoiding the mis-alignment between the gate electrode and the S/D. This structure allows us to directly compare the mobility of n- and p-channel MOSFETs in the same device, because this device works as both n-MOSFET in V_g>0 and p-MOSFET at V_g<0, owing to metal S/D and thin body structure. It should be noted, however, that the resistance at the source and drain region (R_{sd}), due to Schottky barrier at the metal/Ge interfaces, significantly affect the total resistance of MOSFETs and the resulting drain current.

In order to eliminate this effect of R_{sd} in the mobility extraction, 4-terminal Kelvin pattern MOSFETs, shown in Fig. 2, were used. This device has two voltage measurement terminals to measure the voltage drop (V_m) across the channel region with the length of L_m. As a result, the mobility without any effects of R_{sd} can be evaluated by

$$\mu_{eff}(V_g) = \frac{L_m}{W} \cdot \frac{I_d(V_g)}{V_m} \cdot \frac{1}{\int_{V_{th}}^{V_g - V_{mc}} C(V_g) dV_g}$$

where $C(V_g)$ is C-V curves between the gate and the channel and V_{mc} is the potential at the center of the channel.

3. Results and Discussions

Fig. 3 shows I_d-V_g curves with L=50μm. It is clearly observed that the device is working as an n-MOSFET in V_g>0 and as a p-MOSFET in V_g<0 by using the same MOS interface. In order to check the influence of R_{sd}, the relation between V_m and V_g was evaluated (Fig. 4). Note that V_m is the voltage across the half of the channel resistance (R_{ch}). Much smaller V_m in the n-channel than in the p-channel means that R_{sd} in the n-channel is much higher than that in the p-channel. This result is consistent with the fact that the Schottky barrier height of PtGe with n-Ge is much higher than that with p-Ge [9].

In order to examine whether the mobility is accurately determined or not, the mobility was extracted with different V_d and L. Fig. 5 and 6 show the V_d dependence with L=50μm and the L dependence with V_d=0.8V of the electron mobility against E_{eff}, respectively. No V_d and L dependencies of the mobility confirm that the influence of the parasitic resistance is properly eliminated and the channel mobility is accurately evaluated. It is also found that the actual electron mobility of the Ge n-MOSFET without any parasitic resistance effects is almost equal to the Si universal electron mobility.

On the other hand, the hole mobility in the p-channel in the same device is shown in Fig. 7. It is confirmed in p-MOSFETs that the hole mobility is hardly affected by R_{sd}, because of the much lower barrier height. In the present device, however, the hole mobility in p-channel is lower than the Si universal hole mobility. This mobility reduction is attributable to lower crystallinity of the GOI layer and/or poor quality of the MOS interface between the GOI layer and BOX. The above facts that the electron mobility is almost the same as the universal one in spite of the comparatively low hole mobility mean that the low electron mobility, reported so far in Ge n-MOSFETs, is not caused by any inevitable physical reasons. It could rather be expected to provide much higher electron mobility by improving the crystallinity of the Ge channels and the MIS interface properties.

4. Conclusion

In this study, we have established the method of accurately measuring the channel mobility in metal S/D MOSFETs without any effects of parasitic resistance associated with metal S/D junctions. It has been

demonstrated, for the first time, that the electron and hole mobility can be evaluated in the same MOSFETs and the same MOS interfaces by using metal S/D GOI MOSFETs. As a result, it has been found that the present Ge n-MOSFET has almost the same electron mobility as the Si universal one in spite of the comparatively low hole mobility. This fact strongly suggests that much higher electron mobility is expected by further improvement of the material and interface qualities.

Acknowledgements

References

[1] P. Zimmerman et al., IEDM p. 655 (2006) [2] D. Kuzum et al, IEDM, p.723 (2007) [3] N. Taoka et al., APL 92, 113511 (2008) [4] Martens, EDL, 27, p. 405 (2006) [5] H. Shang et al., EDL, 24, p.242 (2003) [6] T. Maeda et al., EDL, 25, p. 102 (2006) [7] S. Dissanayake et al., ICSI-5, p. 57 (2007) [8] S. Nakaharai et al., APL, 83, p.3516 (2003) [9] K. Ikeda et al., Thin Solid Films, 508, p. 359 (2006)
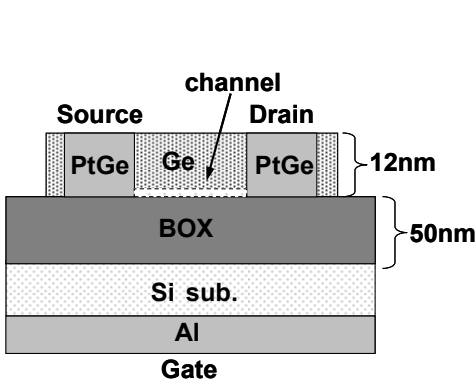

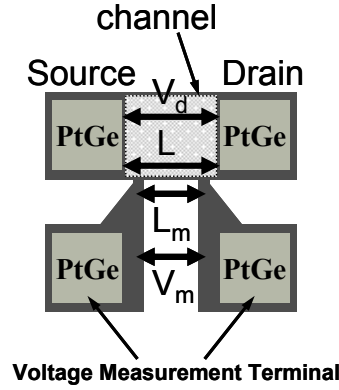Fig. 1 The device structure of metal source/ drain GOI MOSFETs with back gate

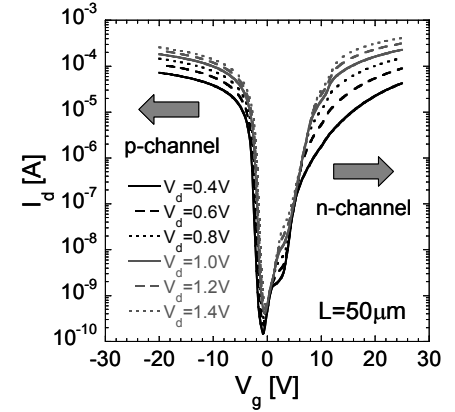Fig. 2 The layout of the device used for this measurement
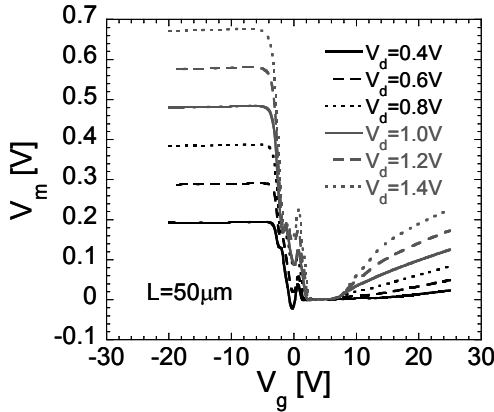

Fig. 3 I_d-V_g curves of MOSFET with L=50μm.

Fig. 4 V_m versus V_g with L=50μm. V_m is larger because of smaller R_{sd} under pMOS operation in V_g<0, while V_m is much smaller because of high R_{sd} under nMOS operation in V_g>0.
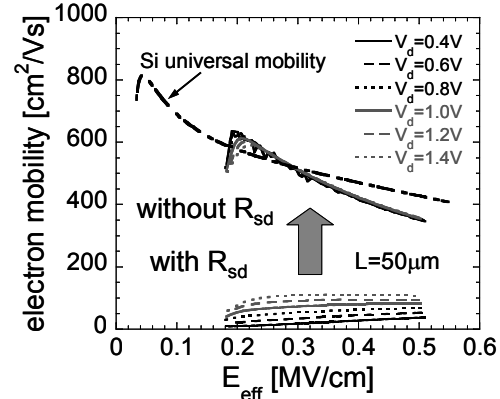

Fig. 5 V_d dependence of electron mobility extracted in the n-channel with L=50μm against E_{eff}. The actual mobility of Ge n-channel is equal to Si, when eliminating the influence of parasitic resistance. There is no V_d dependence.
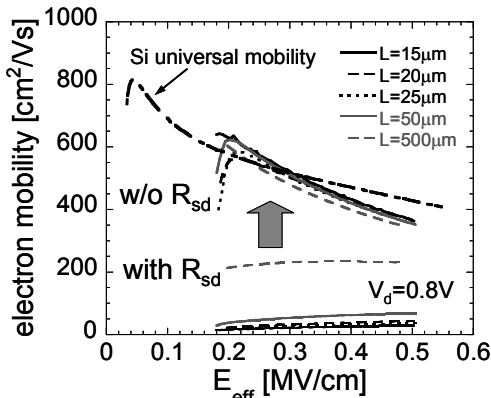

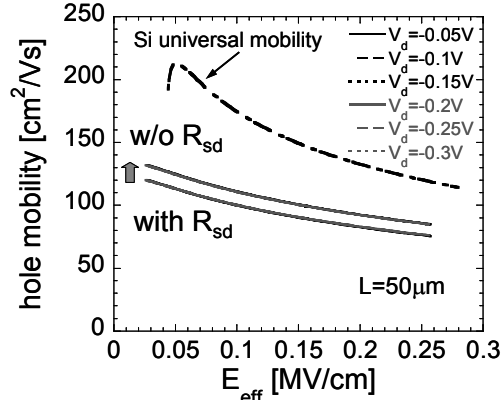Fig. 6 L dependence of electron mobility in n-channel with V_d=0.8V versus E_{eff}. There is no L dependence.

Fig. 7 Hole mobility in p-channel in the same device with L=50μm. The hole mobility has almost no change even after eliminating the influence of parasitic resistance. The hole mobility is smaller than the Si universal one.