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Extending the Bandwidth and Functionality of High Performance InP HBT Technologies

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1. Introduction

InP-based transistor technologies, both high electron mobility transistors (HEMTs) and double heterojunction bipolar transistors (DHBTs), have demonstrated the highest reported transistor RF figures-of-merit. Both device technologies have been reported with current gain cutoff frequencies (f_t) in excess of 600GHz [1,2], and power gain cutoff frequencies (f_{max}) in excess of 1THz [3,4]. These performance records are achieved because of the inherent advantages of the InP/InGaAs material system (high electron mobilities/velocities, low attainable Ohmic contact resistivities and large heterojunction offsets), and through aggressive transistor scaling.

With their wideband gap InP collector InP DHBTs offer a higher breakdown voltage than InGaAs-channel HEMTs at the same f_t. Their high-speed and high-voltage handling make HBTs suitable for a wide breadth of applications including: sub-mm-wave and THz frequency integrated circuits, >100Gbit/sec optical and wireless communication circuits, microwave operational amplifiers, and high resolution microwave frequency analog-to-digital and digital-to-analog converters.

In this paper, we review HBT and IC results from Teledyne Scientific Company's InP HBT technology. A scalable device architecture has been developed and successive generations of the technology have been demonstrated (500nm to 130nm). Increased functionality of the technology is being pursued with the development of a BiFET (HBT+HEMT) InP technology and through heterogeneous integration with Silicon CMOS.

2. HBT Technology

Device Technology

General scaling laws for increasing the bandwidth of InP HBTs have been outlined in [5]. Key technological requirements for the scaling the technology are achieving successive reductions in emitter and base contact resistivities, and developing self-aligned process flows that can support high levels of yield and integration.

At Teledyne, we have developed an HBT process that utilizes dielectric sidewall spacers for forming a self-aligned base-emitter junction. A key attribute of the process is an Au-based electroplating process that forms the emitter contact/post. The electroplating process produces a contact with straight sidewalls and a large height-to-width ratio, attributes that are beneficial to the self-aligned sidewall spacer process. Figure 1 shows the cross-section of a 500nm device after base contact formation.

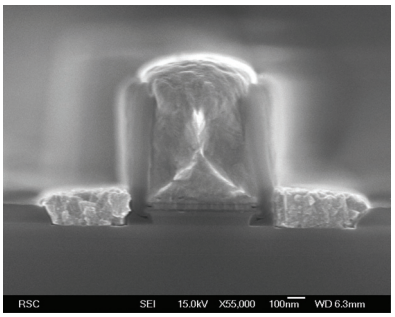

Fig. 1. Cross-section of self-aligned base-emitter junction from Teledyne 500nm HBT process [6]

Table 1: Summary of results from Teledyne's InP HBT process for different generations of emitter junction scaling (W_E)

Parameter	W_E = 500nm [6]	W_E = 250nm [7]	W_E = 130nm [4]
Peak f_t	330GHz	430GHz	520GHz
Peak f_{max}	350GHz	1.0THz	1.15GHz
J_{max} (Peak RF)	5mA/μm²	11mA/μm²	26mA/μm²
BV_{CEO}	4.5V	4.3V	3.5V
Demonstrated Integration Levels (# of HBTs)	1000's	100's	10's

Table 1 summarizes device results from Teledyne HBT technology at different scaling generations. Details of the 500nm, 250nm, and 130nm process technologies can be found in [6], [7] and [4], respectively. The 500nm technology utilizes I-line optical lithography for all process steps, while the 250nm and 130nm technologies use electron beam lithography for emitter contact definition and optical lithography for the remaining process steps. The technology is supported by a multi-level thin-film wiring environment that utilizes a low-κ dielectric (Bezocyclobutene ε_r = 2.7) is utilized with electroplated Au interconnects. A 4-level wiring stack with 2μm ILD thicknesses is used for digital and mixed-signal ICs; however; a modified process with a thicker (>5μm) top-most dielectric has also been developed to provide low-loss microstrip for sub-mm-wave MIC applications [7].

The 500nm process has been utilized to realize ICs with transistor counts >5000. With further maturation of the

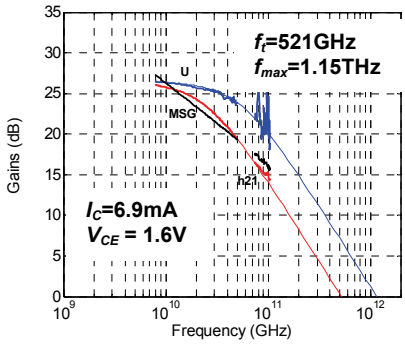

Fig. 2. Measured short circuit current gain (H_{21}) and Unilateral power gain (U) of 0.13x2μm^2 InP HBT [4].

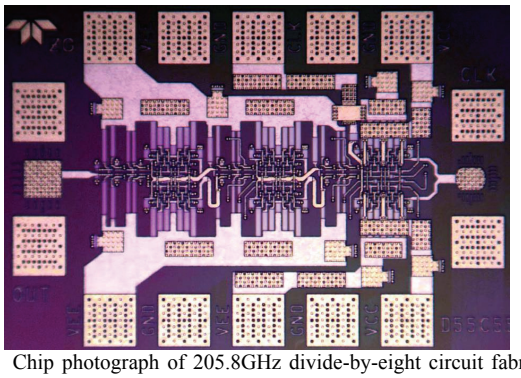

Fig. 3. Chip photograph of 205.8GHz divide-by-eight circuit fabricated in 250nm HBT process. [11]

250nm and 130nm processes, similar levels of integration should be achievable. Fig. 2. shows the measured transistor gains of a 0.13 x 2μm^2 HBT biased for peak RF performance. The HBT exhibits a peak f_t of 520GHz and a peak f_{max} of 1.15 THz.

IC Results

LSI (>3000 HBTs) circuits operating at GHz clock rates have been demonstrated in our 500nm HBT process. These results include direct digital synthesizer circuits operating at >20 GHz clock rates [8], and microwave digital-to-analog converters with >50dB SFDR at 8GHz output [9]. High performance microwave op-amp circuits have also been demonstrated in the technology exhibiting a 30GHz loop bandwidth with an OIP3 of 54.1dBm at 2GHz with ~1W DC power dissipation [10].

The 250nm HBT technology has demonstrated ICs at lower levels of integration but with record performance. These demonstrations include the fastest reported static frequency divider (f_{clock} = 205.8GHz) [11] (Fig. 3). The technology has also been used in the development of new classes of sub-mm-wave and THz frequency monolithic integrated circuits. These demonstrations include: a two-stage cascode amplifier with 20dB gain at 315 GHz [12], fundamental oscillator circuits operating to >500GHz [13], and dynamic frequency dividers operating to >325GHz [14]. Larger levels of complexity have been demonstrated with phased locked loop circuits operating at 220GHz [15] and 300GHz [16].

The 130nm technology has been developed targeting THz integrated circuit results at >600GHz. Results from these efforts will be reported in the near future.

3. InP HEMT and Si CMOS Integration

The high speed and high breakdown attributes of InP HBTs offer an excellent complement to other device technologies. Recent efforts have examined the integration of HBTs with InP HEMTs [17] and Silicon CMOS [18] to increase the functionality of IC platforms. In [17], 35nm InGaAs-channel HEMTs were integrated with 500nm InP HBTs and both devices were demonstrated with f_{max} of greater than 300GHz. In this approach, the HEMT layer was grown first beneath the subcollector of the HBT. Integration with Silicon CMOS has been pursued under the DARPA COSMOS program [18]. Latticed engineered

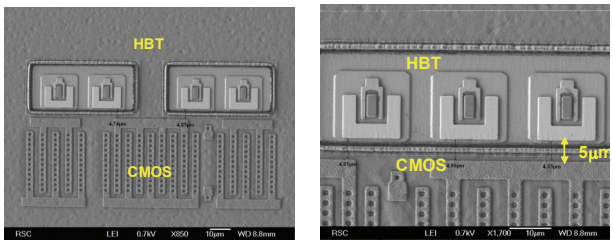

Fig. 4. SEM image of InP HBT integrated with silicon CMOS on silicon wafer [18]

SOI-type substrates are used with a buried Germanium layer that is used as a template for III-V MBE growth after CMOS fabrication (Fig. 4). In both integration schemes (HEMT and CMOS), HBT performance is limited by thermal constraints. Methods of improved heatsinking or eliminating high thermal resistance paths under the HBT are required to integrate the highest performance HBTs.

Acknowledgements

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