Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp530-531

Low-loss Si waveguides with Variable-Shaped-Beam EB Lithography for Large-Scaled Photonic Circuits

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Abstract

We have established low loss of single-mode Si waveguide fabrication process with variable-shaped-beam (VSB) EB lithography. The attenuation loss and bending loss are 1.5dB/cm in 480nm x 220nm core dimension and 0.08dB/turn in 4μm bending radius, respectively. This technology consists of multiple exposure technique using pattern segmentation software and EB lithography technology with lower line edge roughness (LER) and controlled high resolution process conditions.

1. Introduction

Silicon photonics research has been conducted to break through the technology limitation of data transmission rate in LSI. To attain the target, it is considered that the establishment of lithography process for low LER and well-controlled CD is the most critical factor in device fabrication. Thus VSB-EB lithography is a one of suitable fabrication method that enables photonic device with its high resolution, mask-less feature, and more than 10-times faster in throughput than point-beam EB. However, there are several concerns that we have to come over on VSB-EB lithography technique. Those are inherent field stitching error and stepwise distortion in bend shape profile due to rectangle shaped beam. [1-2]

In this paper, we present newly developed VSB-EB lithography technology, which improves the writing performance of stitching error and bend shape. And, we examine the suitability of the EB lithography technology to Si photonics devices by through the results of waveguide characteristics.

2. Data preparation and multiple exposure technique in VSB-EB lithography

In this section, we describe the EB methodology that reduces the stitching error and the distortion in bend shape. The EB draw data processing procedure is shown in Fig.1. Firstly, the curved polygon outline in GDS data was smoothed with interpolation. Then, narrow rectangles (typically 20nm in short side) were allocated side by side along with the smoothed arc outline. For multiple exposure, the pattern generation was repeated by numbers of exposure times with shifting the pattern splitting start point. As the results of these procedures, the arc pattern outline was expressed by small step height less than resolution limit of EB resist (Fig. 2-A), and the smoothed arc shape was confirmed with SEM image of resist pattern (Fig. 2-B). By applying multiple exposure technique, the field stitching error, $|Avg.|+3\sigma$ was drastically reduced 27.4nm to 7.9nm (Fig.3) because of averaging effects in e-beam landing position.

3. Optimization of EB resist process

In this investigation for EB lithography technology, we used ADVANTEST F5112 as VSB-EB writer. As an EB resist material capable to the waveguide core processing, a negative tone resist, TOK OEBR-CAN034 was selected. Electro-conductive top coating was applied in order to discharge the electrically charged wafer. Line width and LER was measured with Hitachi S-9260A CD-SEM. **Fig.4** shows the temperature dependence of LER in post exposure bake (PEB). LER and its uniformity are varied with the PEB conditions. We obtained the LER 1.9nm ± 0.2nm within a wafer as the result of resist process optimization. Also, applying this resist process condition and taking into account of proximity correction, we examined the higher resolution capability. **Fig.5** shows the highest 30nm resolution for isolate lines with less than +/-10nm linearity error. As shown in **Fig.6**, CD difference from mean to target is well controlled for line patterns of various ration of line-to-space

4. Si waveguide characteristics

In this section, we describe the optical characteristics for waveguides fabricated by using 4inch SOI wafers with 3μm buried oxide (BOX). The process is as follows. At the first step, a thin oxide film was grown on the top of the SOI, which act as a hard mask for Si etching. On the top of the oxide-coated SOI, resist patterns was formed by 4-times multiple EB exposure. The tact time for multi-exposure to a single waveguide pattern of 37mm length with 10 arcs was estimated to be less than 1min. SOI layer etching was carried out with CHF_3 based oxide-etch and following that HBr based main-etch. Post etching resist was removed by dry ashing and wet process. Finally, 2μm plasma TEOS film was deposited as an overclad. The fabricated waveguide dimension was 460-500nm in core width and 220nm in height. The CD errors for core width were less than +/-10nm in width.

Fig. 7 shows the core width dependency of attenuation loss for λ=1.55μm measured by cut-back method. The attenuation loss varied from 1.3 to 1.5dB/cm and no

significant core width dependency was observed. Such small dependency implies that, in our low-loss waveguide, LER controlled at a low level might not be the main cause for propagation loss. Another advantage of this process was bending loss improvement which is seen in Fig. 8. The bend loss is less than 0.1dB/turn for greater than 4μm bending radius.

5. Conclusion

We have successfully established low-loss Si waveguides fabrication process applicable to large-scaled photonic circuits, by using advanced VSB EB lithography technology.

Acknowledgements

This research is partly granted by JSPS through the FIRST Program initiated by CSTP, and conducted at TIA-SCR. The author is deeply grateful to Dr. K. Yamada, Mr. H. Yaegashi, Mr. D. Shimura, PECST, for useful discussion, and to Mr. N. Doumae and Mr. J. Higasa, Advantest Corp., for their technical discussion and supports to the development of multiple exposure technique.

References

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[2] T. Horikawa et.al., Proc. of 57th JSAP (2010); N. Hirayama et.al., Proc. of 58th JSAP (2011)

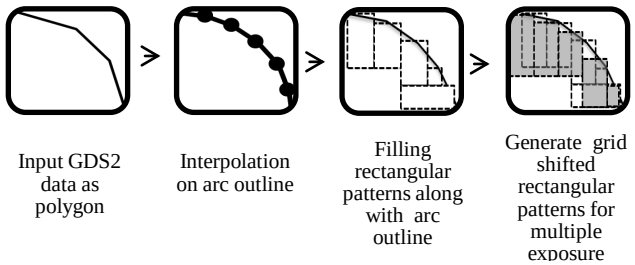

Fig.1 Schematic processing procedure for pattern segmentation to an arc.

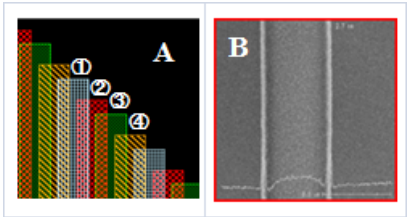

Fig.2 (A) EB drawing data image for arc pattern by developed data preparation software (Overlapped 4-times multiple exposure data) and (B) SEM image of arc pattern with multiple exposure.(Image is rotated 45degrees in clockwise direction)

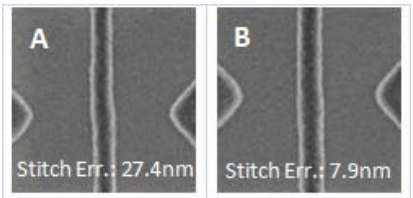

Fig.3 SEM images of field stitching error: (A) single exposure, (B) 4-times multiple exposure. Measured stitch error is inserted on each image.

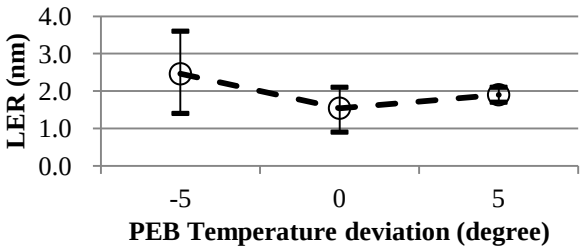

Fig.4 The dependence of LER in resist line pattern on temperature in Post-exposure-bake (PEB).

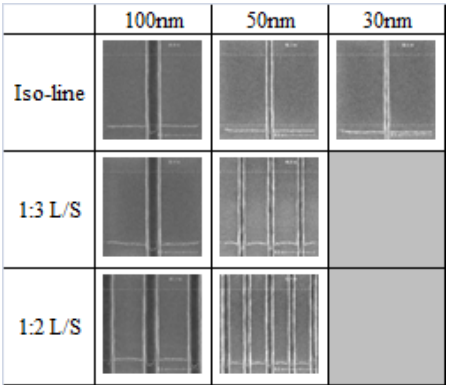

Fig.5 Resolution chart for EB resist pattern in isolated line, 1:3 line and space, and 1:2 line and space.

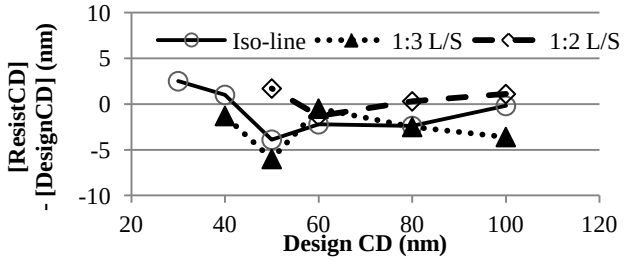

Fig.6 The CD errors from designed CD in EB resist line width for isolated line, 1:3 line-and-space, and 1:2 line-and-space.

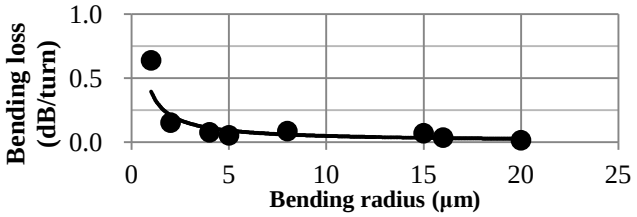

Fig.7 The dependence of bending loss on bending radius for Si waveguides with 460nm x 220nm core dimension.

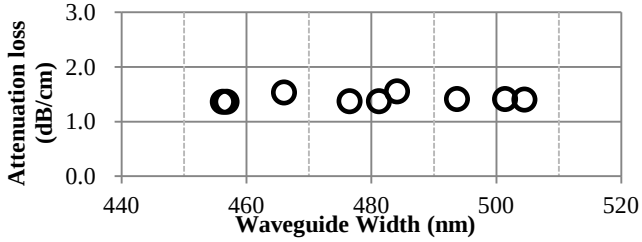

Fig.8 The dependence of attenuation loss on waveguide width for TE mode propagation in fabricated Si waveguide of 220nm in height.