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New erase verify scheme for improving the cycling endurance of 2xnm NAND flash cell

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1. Introduction

As the NAND flash memory cells are scaled down, there are serveral obstacles, such as retention, endurance, distribution widening, disturb. In order to overcome those problems intrinsically, the reducing interface and bulk traps in tunneling oxide are required. Because these traps are generated by FN (Fowler-Nordheim) tunneling during P/E (Program/Erase) operation, the reduced FN stress is one of the key factors to achive better reliability. After P/E operation, the traps make cell V_T (threshold voltage) positive [1], [2]. It means that the program voltage can be reduced, but the erase bias should be increased.

During erase operation, erase status is checked by applying the same voltage on the entire gate (Verify V_T). If verify V_T is larger than targeting erase V_T, additional erase bias is applied with ISPE operation (Incremental Step Pulse Erase). In general, the increasing erase bias is similar with erase V_T shift after P/E cycle. However, we found out that the increasing erase bias is more than erase V_T shift (Fig 1) in our chip test.

In this work, we investigate a reason why the applied erase bias increases more than erase V_T shift and propose a new erase verify scheme for reducing erase bias by using gradual WL voltage.

2. Analysis of the erase bias

For analysis of increasing erase bias phenomenon, the V_T distribution of erased cell is measured in our NAND flash cell of 2xnm node [3]. As shown in Fig. 2 (a), the erased cell V_T distribution after P/E cycle shows wider than initial one, and it induces the increased erase more than erase V_T shift since the erase verify operation needs an erase bias enough to pass right-tail of distribution. In order to find out the causes of the slow erased cell in right-tail region of V_T distribution, we tracked cells and extracted its I_d-V_G curves (Fig. 2 (b)). The trans-conductance of tracked slow cells shows much worse characteristics as the V_T distribution is closer to right-tail, and it means that the slow cells are degraded by the injected interface traps during P/E cycle [2]. In addition, the non-uniform distribution of the interface traps is generated at the gate-edge region than the center [4]. Based on these models, we can get the very well matched I_d-V_G characteristics with the experimental data as shown in Fig. 2(b) using TCAD simulation.

3. New erase verify scheme and results

During erase operation, the cell V_T after P/E cycle moves to positive direction because of traps in tunneling oxide and it means that the additional erase pulses are required to pass the verify V_T, and it induces worse reliability characteristics due to the increased erase stress. According to this sequence, we need to reduce the erase verify voltage to get the reliable cell. In order to find a way for reducing positive verify V_T shift, erase verification was simulated.

The Fig. 3 shows the simulated potential profile before and after P/E cycling in NAND cell string. The surface potential drop of the source-side channel is much severe than drain side. This phenomenon can be a one of the reasons for increasing positive verify V_T shift, because it can restrict an injection of electron from source.

From this analysis, we can propose a new erase verify scheme to improve reliability characteristics by compensating the surface potential drop of the source-side channel using the increased gate voltage from center WL to the source-side WL gradually (Fig. 4). As shown in Fig. 5, the verify V_T shift after P/E cycle can be decreased by using this scheme. When we increase the gradient of gradual gate voltage, we can get much better results to reduce the verify V_T shift. Reducing of the verify V_T shift is saturated in gradient of gradual gate voltage 0.8V per WL from center to source-side WL. In our study, the estimated improvement of cycling endurance is about 20% in that case. The Fig. 6 shows the source-side channel surface potential with the various gradual gate voltages. In case of gradual gate voltage in gradient of 0.8V per WL, there is nearly no source-side channel potential drop and it is the reason why improvement of verify V_T shift is saturated.

4. Conclusion

New erase verify method for improving the reliability characteristics is proposed. By using new erase verify scheme, we can reduce verify V_T shift by compensating source-side channel surface potential drop and improve about 20% endurance in our estimation.

References

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[2] J. D. Lee, et al, *2004 IEEE Transactions on Device and Materials Reliability* (2004) 110-117
[3] K. W. Lee, et al, *2011 Symposium on VLSI Technology Digest of Technical Papers* (2011) 70-71.
[4] A. Fayrushin,et al, *2009 Electron Devices Meeting (IEDM)* (2009) 34.2.1-34.2.4

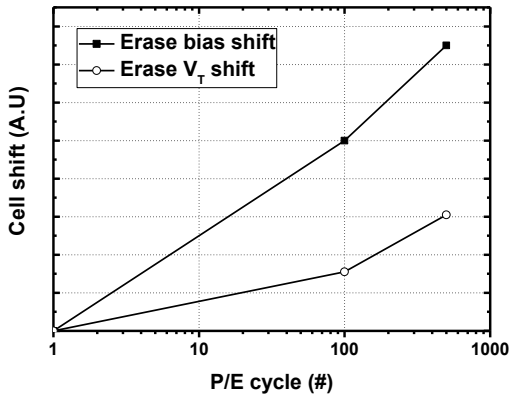
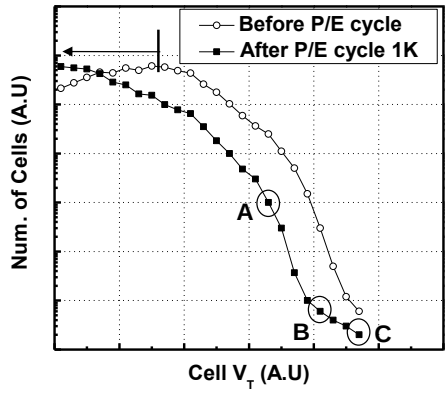
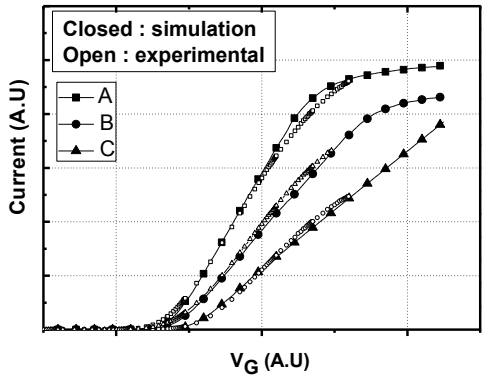


Fig. 1 Erase V_T and erase bias shift with P/E cycle

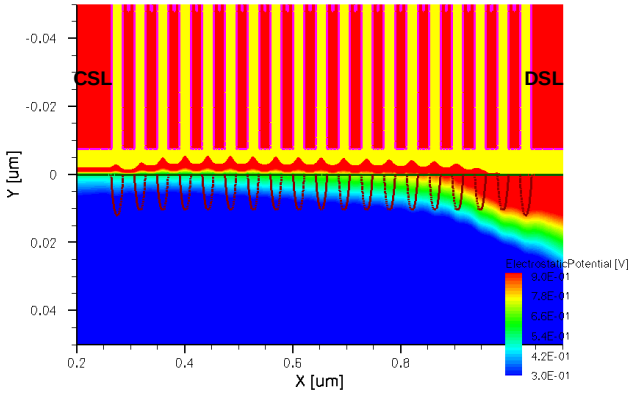


(a)

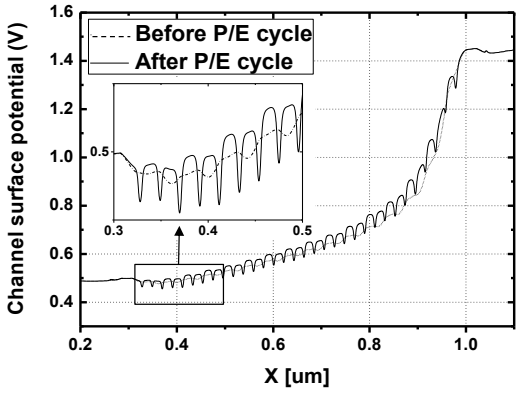


(b)

Fig. 2 (a) Erased cell distribution before and after P/E cycle and (b) cell I_d-V_G curves of slow erased cell in right-tail of distribution and correlated simulation results



(a)



(b)

Fig. 3 (a) Electrostatic potential and (b) channel surface potential during erase verification before and after P/E cycle.

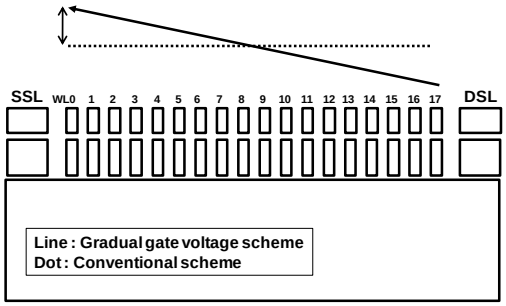


Fig. 4 New erase verify scheme with increasing source-side gate voltage to compensate source-side channel surface potential drop after P/E cycle.

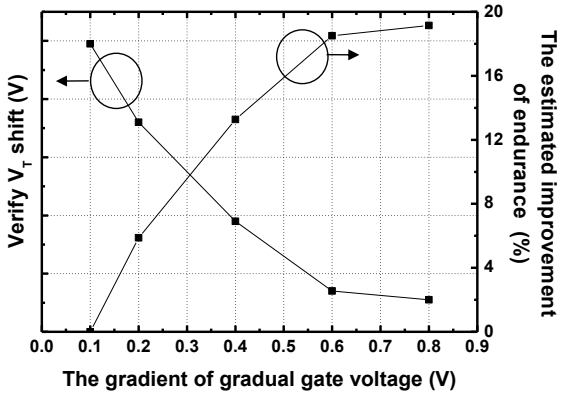


Fig. 5 The simulated verify V_T shift with various gradual gate voltage and the estimated improvement of endurance.

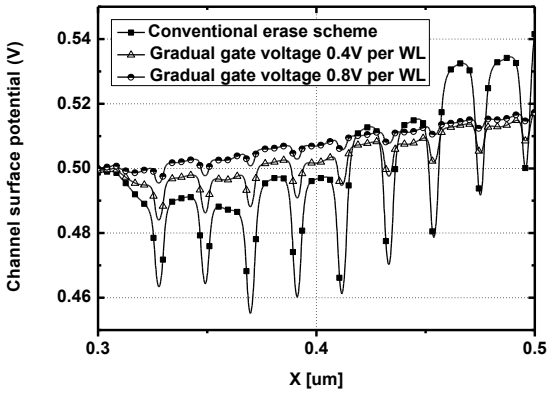


Fig. 6 Source-side channel surface potential with various gradual gate voltages after P/E cycle.