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Chemical Vapor Deposition $GeTe/Sb_2Te_3$ Super-Lattice Phase Change Memory

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Abstract

This paper describes the fabrication and electrical properties of a CVD $GeTe/Sb_2Te_3$ Super-Lattice Phase Change Memory. We present its excellent crystal structure and non-volatile operations for the first time in this paper.

1. Introduction

A $GeTe/Sb_2Te_3$ Super-lattice Phase Change Memory (SL PCM) has been extensively investigated as the next generation of non-volatile memory. SL was proposed by J. Tominaga [1, 2], and it is composed of thin GeTe and Sb_2Te_3 films. The GeTe is aligned in the direction of the c-axis of the Sb_2Te_3 in SL. This results in the short-range motion of the Ge atoms for changing the resistance states (Fig. 1). A crystal-to-crystal change occurs in SL, which leads to a reduction in the write energies to less than 1/10 that for conventional GeSbTe [3, 4].

On the other hand, not only the Physical Vapor Deposition (PVD) but also Chemical Vapor Deposition (CVD) of phase change materials have been investigated [5,6] to increase the bit density of PCM. In the long run, we believe that CVD SL will become a key factor for continually increasing the density of PCM. This paper presents a new CVD fabrication process for SL PCM. Set and reset characteristics with good cycling endurance of 1E+5 times is also presented.

2. $GeTe/Sb_2Te_3$ CVD on 300-mm Si wafer

The main concerns when fabricating CVD GeTe / Sb_2Te_3 SL are the thickness and roughness of it (Table 1). This work improved them by using a method that combines the synchronized and unsynchronized precursor supplies (Fig. 2). This method was developed to fabricate GeTe and Sb_2Te_3 using an identical deposition temperature. The SL films were deposited on Φ300-mm Si wafers (Table 2). A bubbling method was used for the supply system of the precursor, and nitrogen was used as the purge and carrier gases.

Thin Sb_2Te_3, GeTe, and GeSbTe CVD films were successfully fabricated using precursor molecules with planar structures (Fig. 3). The composition of Sb-Te was dependent on the Te precursor flow, and Sb_2Te_3 was created using a Te precursor flow rate of 30 cc (Fig. 4). The contaminants in the film were below the detection limit of XPS (Fig. 6). We also successfully created GeTe using a 3.6-cc Ge precursor flow rate (Fig. 5). These films were deposited at a temperature of 250 deg. (Figs. 7 and 8).

Table 3 lists the XRD and TEM measurement results from the GeSbTe and $GeTe/Sb_2Te_3$ CVD films. The XRD data from the $GeTe/Sb_2Te_3$ CVD film had peak shifts in the hexagonal Sb_2Te_3. These peaks were different from those of GeSbTe, and were caused by the c-axis orientation of GeTe on Sb_2Te_3. Therefore, they indicate the formation of SL [4]. The TEM data showed atomic interference fringes, and those of the SL looked narrower than those of GeSbTe.

3. Non-volatile Operation of CVD $GeTe/Sb_2Te_3$

We fabricated 2-terminal device implementing CVD $GeTe/Sb_2Te_3$ SL films. There were eight CVD $GeTe/Sb_2Te_3$ SL film periods, and the total thickness was 56 nm. The contact size was 100 nm in diameter. Figures 9 and 10 show the reset and set programming characteristics, respectively. The pulse timings (trailing edge/width/falling edge) were 5/100/5 nsec for the reset operation and 100/700/1000 nsec for the set operation. A non-volatile recording between $R_{reset} > 2$ MΩ and $R_{set} < 30$ kΩ was successfully confirmed at a resistance ratio of more than 10. Repeated operations at a 1E+5 cycling endurance were demonstrated (Fig. 10).

4. Further Improvement

We believe further improvement, such as longer endurance and lower set and reset voltages, would be possible by optimizing the thickness of the $GeTe/Sb_2Te_3$ SL films.

5. Conclusion

CVD $GeTe/Sb_2Te_3$ Super-lattice phase change memory was created for the first time. The results from our XRD and TEM measurements verified that the synchronized and unsynchronized supply of precursors made it possible to deposit a $GeTe/Sb_2Te_3$ super-lattice. We demonstrated a non-volatile SL CVD operation with a 1E+5 cycling endurance.

Acknowledgements

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[2] R. E. Simpson et al., *Nature Nanotech.*, **6** (2011) pp. 501-505.
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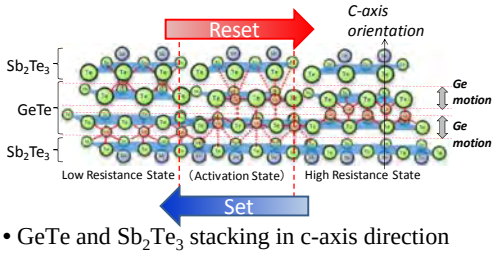


- GeTe and Sb_2Te_3 stacking in c-axis direction
- Crystal_to_crystal change (short-range Ge motion)

⇒ reduction of operational power

Fig. 1 GeTe/Sb_2Te_3 Super-Lattice films[1]

Table 1 Main concern for GeTe/Sb_2Te_3 CVD.

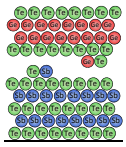
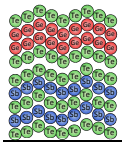
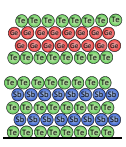
concern	thickness	roughness	ideal
supply of precursors	Synchronized	Unsynchronized	Synchronized + Unsynchronized
GeTe/Sb_2Te_3 Stacking			
deposition temperature	$T_{GeTe} \neq T_{Sb2Te3}$	$T_{GeTe} \neq T_{Sb2Te3}$	$T_{GeTe} = T_{Sb2Te3}$

Table 2 CVD process conditions.

deposition temperature	Max. 400 deg
wafer size	300 mm
supply system	bubbling
purge gas	N_2
carrier gas	N_2

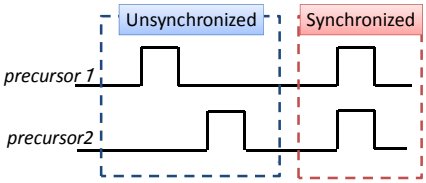


Fig.2 Supply sequence of precursors. Synchronized and unsynchronized sequence were combined.

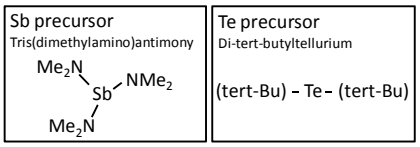


Fig.3 Sb and Te precursor molecules with planar structures.

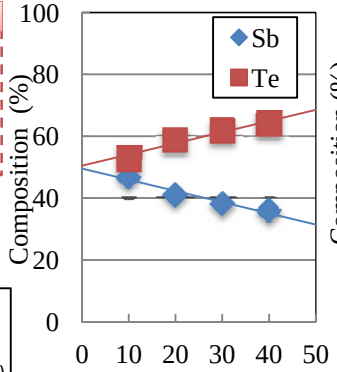


Fig. 4 Sb-Te CVD. The Sb_2Te_3 was successfully obtained using 30 cc of Te precursor.

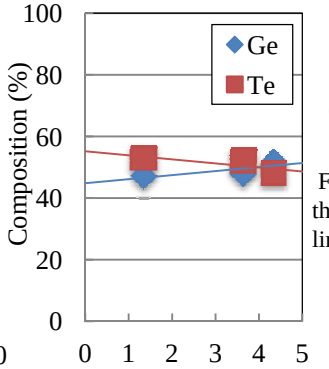


Fig.5 Ge-Te CVD. The GeTe was successfully obtained using 3.6 cc of Ge precursor.

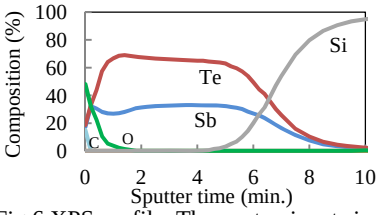


Fig.6 XPS profile. The contaminants in the Sb-Te film were below the detection limit.

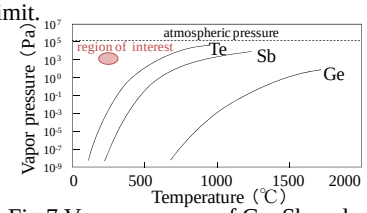


Fig.7 Vapor pressure of Ge, Sb and Te. Region of interest was near 1000 Pa and 250deg.

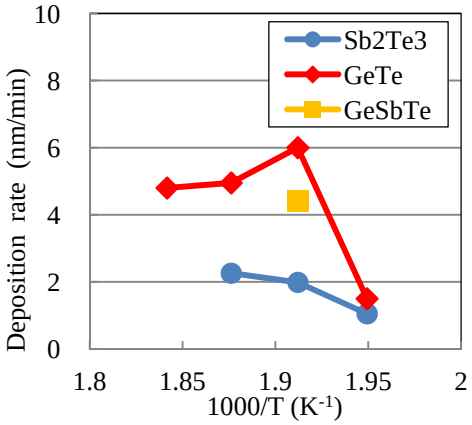
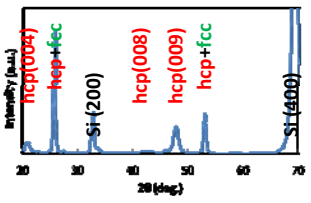
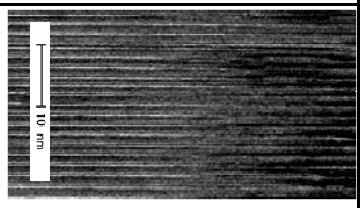
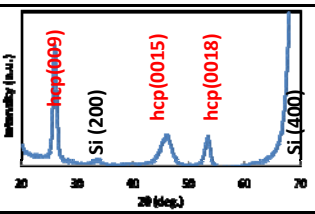
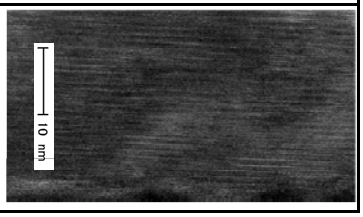


Fig.8 CVD deposition rates. It became possible to deposit Sb_2Te_3, GeTe, and GeSbTe at an identical temperature of 250 deg.

Table 3 XRD and TEM measurement results for GeSbTe and GeTe/Sb_2Te_3 CVD films.

crystal	XRD	TEM
GeSbTe hcp+fcc		
GeTe/Sb_2Te_3 hcp		

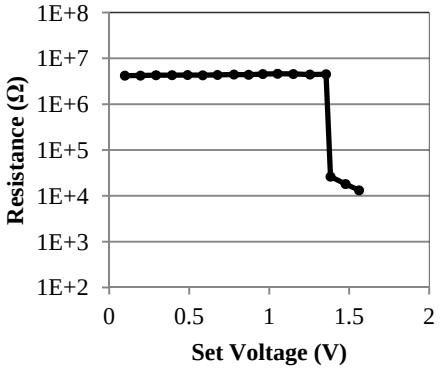


Fig. 9 Set operation of CVD GeTe/Sb_2Te_3 SL device. We used a set pulse with a trailing edge/widths/falling edge = 100/700/1000 ns.

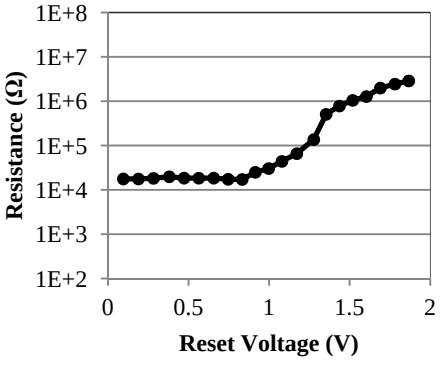


Fig. 10 Reset operation of CVD GeTe/Sb_2Te_3 SL device. We used a reset pulse with a trailing edge/widths/falling edge = 5/100/5 ns.

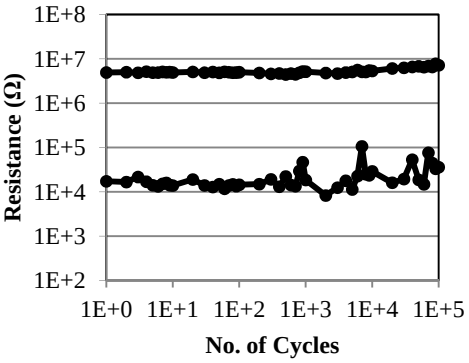


Fig.11 Reset/set cycle operation of CVD GeTe/Sb_2Te_3 SL device.