Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp588-589

Pulsed operation of resistance switching memory of $Si/CaF_2/CdF_2$ resonant-tunneling quantum-well structures

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Abstract:

A novel scheme of resistance switching memory (ReRAM) using $Si/CaF_2/CdF_2/CaF_2/Si$ resonant-tunneling quantum-well (QW) structures grown on Si substrate has been proposed and write-erase cyclic memory operation has been demonstrated at room temperature for the sample with thickness of 0.93/0.93/2.5/0.93 nm for respective layer sequence of $Si/CaF_2/CdF_2/CaF_2$ heterostructure grown on Si(111) substrate. Periodic pulsed operation corresponding to write-read-erase-read memory cycle more than 4500 cycles with 2 ms-width pulse sequences have been successfully observed.

1. Introduction

The dimension of the elements consisting integrated circuits is going down into nano-scale. One essential building block for nanoscale solid state switching devices is electric potential sequences for controlling electron transport, which can be implemented using energy band discontinuity at atomically abrupt heterointerfaces. A $CdF_2/CaF_2/Si$ heterostructure is an attractive candidate for applications on Si substrates, such as resonant tunneling diodes (RTDs) [1] and transistors [2] coulomb blockade devices, because of the large conduction band discontinuity (ΔE_C~2.9eV) at the heterointerface [3] and small lattice mismatch with silicon. To date, we have demonstrated large ON/OFF current ratio of CdF_2/CaF_2 RTDs larger than 10^5 at RT [4-6], which confirmed advantage of the large ΔE_C heterostructure material systems. Recently, we have proposed and demonstrated novel scheme of resistance switching diode or resistance random access memory (ReRAM) cell using $Si/CaF_2/CdF_2/CaF_2/Si$ quantum-well (QW) structure [7-9]. However, pulsed response and repetitive endurance of the proposed device structures has not been reported yet. In this study, we have investigated periodic pulsed response of the proposed resistance switching memory structure and demonstrated periodic memory cycle operation.

2. Structure and operation principle

Figure 1 shows schematic device structure and band diagram (flat band) used in this study. Basic structure of the device is $CaF_2/CdF_2/CaF_2$ double-barrier resonant tunneling diode combined with quantum-well (QW) structure sandwiched by silicon as the secondary energy barriers. The CaF_2 layers act as energy barriers mainly for charge injection and ejection between a CdF_2 QW and a reservoir of electrons. Si layers act as energy barriers for suppression of electron escape from the CdF_2 QW. Using this layer configuration, write/erase voltages can be controlled by designing the appropriate thickness of CdF_2 quantum-well (2.5 nm-thick CdF_2 QW provides 1 V switching voltage for example) based on resonant tunneling scheme. Injected electrons are retained in the CdF_2 QW because conduction band minimum of CdF_2 is ~0.6eV lower than that of Si therefore retention time can be controlled by the thickness of n-Si barrier layer. In writing operation, electrons are injected from a metal (Al) layer or n-type Si layer by resonant tunneling or sequential tunneling and a part of the electrons are trapped in CdF_2 QW. Trapped electrons are steeply increased at around peak voltage (V_{peak}) because electron injection rapidly increases at around V_{peak}. Therefore, resistance switching occurs at around V_{peak} of a $CaF_2/CdF_2/CaF_2$ RTD. ON/OFF current ratio of more than 1000 can be expected theoretically due to the difference of tunneling probability between charged states and uncharged states of the CdF_2 QW.

3. Experiment

An 80 nm-thick SiO_2 layer was formed on a p-type Si(111) 0.1° off substrate with resistivity of less than 4 mΩ·cm using thermal oxidation at 900°C. Subsequently, 2 μm-diameter holes were formed by photolithography and BHF etching. After loaded into the ultra-high-vacuum (UHV) chamber, a 0.93 nm-thick CaF_2 layer was grown using partially ionized beam technique at substrate temperature T_s=650°C. Subsequently, a 2.5-nm-thick CdF_2 quantum-well layer, a 0.9-nm-thick CaF_2 layer and finally the 0.9-nm-thick Si layer were grown at T_s= 80°C with As flux for dopant using a cracking cell. After unloaded from the UHV chamber, Al/Au electrodes of 200 μm square were formed by lift-off.

4. Results and discussions

In the measurement of memory operation via I-V curve using DC bias sweep, bipolar resistance switching memory cycles have been clearly observed at room temperature. One example of I-V curve was shown in Fig. 2. Switching voltage V_{peak} (voltage for state transition from low resistance state to high resistance state) was 0.82 V, peak current I_{peak}= 7.4 mA and ON/OFF current ratio was around 2.0, while the measurement values of ON/OFF ratio were dispersed in the range of around 1.5–20 by sample to sam-

ple.

Figure 3 shows pulsed response sequence of periodic write-read-erase-read memory cycle operation at room temperature: (a) input pulse voltage sequence and (b) current response. Input pulse voltage for 'write", "read", "erase", "read" were 1.5V, 0.4V, -1.5V, 0.4V, respective sequence with pulse width of 2 ms. As shown in Fig. 3(b), each current pulse for "read" periods clearly corresponds to current of high resistance states ($I_{H.R.S.}$) and of low resistance states ($I_{L.R.S.}$) corresponding to the expected state transition. Figure 4 shows the plots of $I_{H.R.S}$ and $I_{L.R.S.}$ as a function of the number of memory cycles. It has been observed that 4500 periods of memory cycles with perfect separation of $I_{H.R.S}$ and $I_{L.R.S.}$ with no errors.

5. Conclusion

We have studied pulsed response of ReRAM characteristics of Si/CaF_2/CdF_2/CaF_2/Si tunneling quantum-well structures grown on Si substrate. Periodic pulsed response corresponding to write-read-erase-read memory operation more than 4500 cycles has been successfully observed, which is the first report for the device structure proposed in this study.

References

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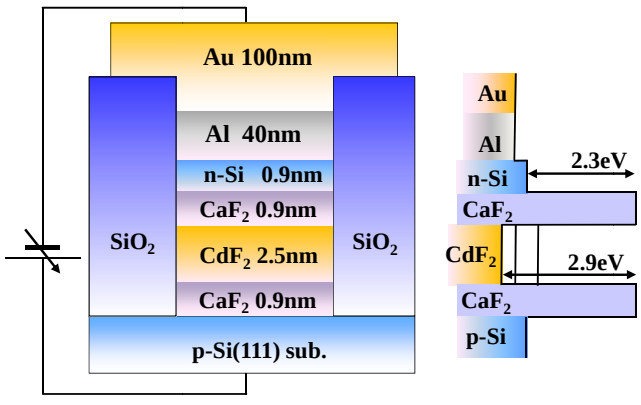

Fig. 1 Schematic device structure and conduction band profile.

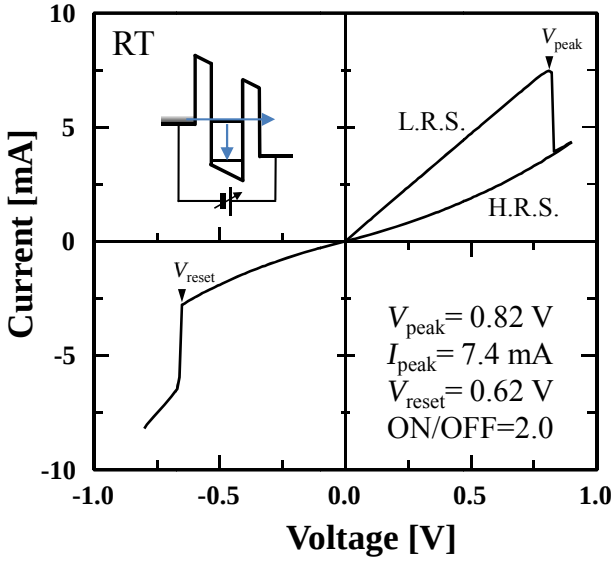

Fig. 2 A current-voltage (I-V) curve of memory cycle operation at room temperature.

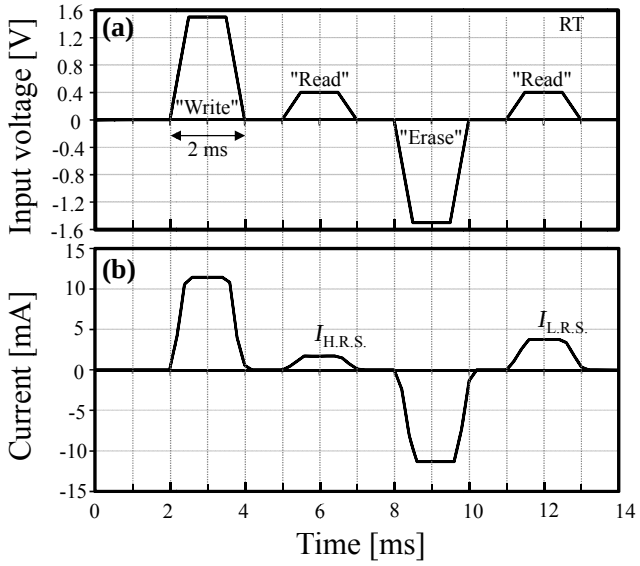

Fig. 3 (a) Time sequence of input pulse voltage of 2ms-width. (b) Corresponding current sequence.

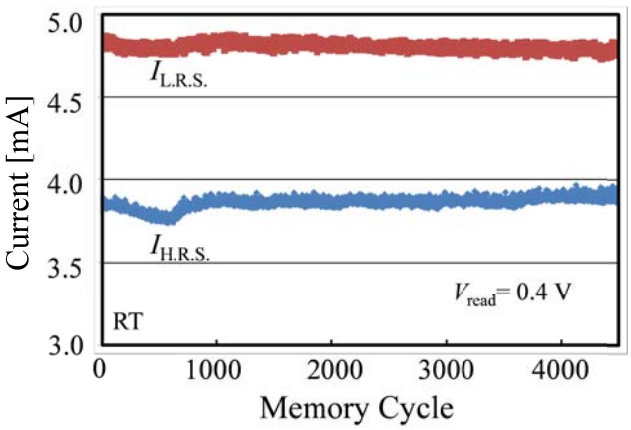

Fig. 4 Plots of current of low resistance states ($I_{L.R.S.}$) and high resistance states ($I_{H.R.S.}$) as a function of the number of memory cycles. Voltage for "read" (V_{read}) was 0.4 V.