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10^8 Endurance Nonvolatile Memory Transistor with 100 nm Metal Gate

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Abstract

High endurance ferroelectric-gate field effect transistors (FeFETs) with 100 nm-long metal gates were successfully produced. An improved fabrication process was applied for downsizing the gate length of the FeFETs with keeping large memory windows of about 1.1 V at V_g = 1±5 V. High endurance of 10^8 cycles and long retention for about 4×10^5 s were confirmed.

1. Introduction

There are many types of developing nonvolatile memories such as ferroelectric-gate field-effect transistor (FeFET) [1,2], STT-MRAM [3], PCRAM [3], ReRAM [2], and so on, which are aiming for commercialized popular memories like FeRAM [3] and flash memories [4]. Among them, the FeFET is a good candidate of a post-flash storage because it has extremely low power consumption as a unit cell [1,2] and also as an integrated circuit of a ferroelectric NAND flash memory [5]. Very recently, a progress in downsizing the FeFET has been made by using an improved fabrication process [6] after we reported a 260 nm-gate FeFET [7]. In this paper we will introduce world the smallest 100 nm-gate FeFET with good performances of 10^8 cycle endurance and a long retention.

2. Fabrication process

Silicon (Si) substrates patterned with active areas including source-and-drain contact regions isolated by local-oxidation-of-silicon were prepared. After removing sacrificial SiO_2 on the active fields by a buffered hydrofluoric acid, 7 nm-thick HfO_2 and 190 nm-thick $Sr_{1-x}Ca_xBi_2Ta_2O_9$ (SCBT (x = 0.2)) layers were sequentially deposited by pulsed laser deposition using a KrF laser controlled at 250 mJ. The HfO_2 and SCBT were deposited in 15 Pa-N_2 at 220 ºC and in 7 Pa-O_2 at 415 ºC, respectively. Pt was deposited to 150 nm by radio-frequency (rf) sputtering on the SCBT. Gate-etching masks were patterned on the Pt by electron-beam (EB) lithography. A negative EB resist was spin-coated by 5000 rpm. Tetra-methyl-ammonium -hydroxide for developer and deionized water for rinse were used. The EB-resist mask patterns were finally made about 500 nm tall. The Pt layer was etched by Ar^+ ion milling and the SCBT/HfO_2 double layers were etched by inductively-coupled-plasma reactive-ion-etching (ICP-RIE, ULVAC CE-300I). The etching conditions for forming the Pt/SCBT/HfO_2 gate stacks of the FeFETs were described in Table 1. By using the fine-shaped EB-resist masks and the well-optimized etching conditions, the gate stacks with metal-gate length (L) and width (W) of L = 100 nm and W = 10 μm were formed. Phosphorous ions (P^+) of the dose 2E+13/cm^2 were implanted by the acceleration energy 10 keV to the gate stacks for making shallow self-aligned sources and drains. Another 50 nm-thick SCBT of x = 0.3 was deposited to cover the gate-stack sidewalls. A metal organic chemical vapor deposition (MOCVD) system (Doctor T^{TM}, WACOM R&D) was used for good coverage of the thin SCBT films. The film thickness was estimated by an ellipsometer. The MOCVD-SCBT film was etched back by the ICP-RIE with anisotropy. The Pt was also etched and became about 120 nm-thick. The second shallow sources and drains were formed by the P^+ implantation of the dose 1E+14/cm^2 by 15 keV. The second implantation was performed to reduce resistance of the source and drain regions and to secure measureable essential drain-current (I_d). The gate stacks were covered with 200 nm-thick SiO_2 passivation layers and finally annealed once at 800 ºC in O_2 for 30 min for the core- and sidewall-SCBT poly-crystallization and implanted P^+ activation. Contact holes for gates, sources, drains and substrates were opened by Ar^+ milling. Schematic structure of the finished FeFET was shown in Fig. 1.

Table 1 Etching conditions for forming the FeFET gate stacks

material	Pt	core-SCBT/HfO_2	sidewall-SCBT
method	Ar^+ milling	ICP-RIE	ICP-RIE
process gas	Ar 4 sccm	Ar 3 sccm +BCl_3 7 sccm	Ar 5 sccm +BCl_3 5 sccm
pressure	0.014 Pa	0.25 Pa	0.25 Pa
etching power	beam voltage 1.1 kV	antenna rf 750 W, bias rf 400 W	antenna rf 600 W, bias rf 300 W

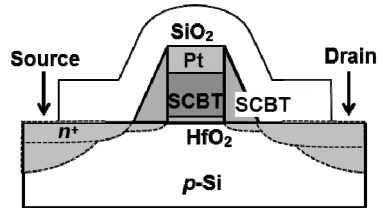

Fig. 1 Schematic cross section of the FeFET produced in this work.

3. Results and Discussions

We previously demonstrated that using the SCBT instead of $SrBi_2Ta_2O_9$ (SBT) as the core ferroelectric material effectively widened the memory window of the FeFET [8].

We also found that coating MOCVD-SCBT on the as-etched gate-stack sidewalls and annealing altogether could recover the FeFET memory windows narrowed by etching damages [6]. In this work, planar FeFETs with L = 100 nm and W = 10 μm metal gates were produced by applying all the improved techniques such as using the SCBT for the core ferroelectric material in the FeFETs, covering the sidewalls by the SCBT films, and etching fine by the optimized conditions. Figure 2 shows the FeFET cross section observed by a focused-ion-beam scanning-electron microscope (FIB-SEM). The cross-sectional surface was formed by 40 keV Ga^+ ion beam and observed in-situ by the 54° tilted SEM from the surface. About 120 nm-thick Pt layer was remained as the gate metal after the sidewall MOCVD-SCBT film was etched back. Note that the photo appeared shrank by a factor of sin54° in the vertical direction only.

Important electric properties of the FeFETs were measured. Drain current-gate voltage (I_d-V_g) curves, I_d-retention and threshold-voltage (V_{th})-endurance properties were characterized using a semiconductor parameter analyzer, a pulse generator and a DC trigger source which were controlled by originally-made NI Labview programs.

The static I_d-V_g curve at V_g scanning range of $V_g = 1 \pm 5$ V showed a wide memory window of 1.14 V at $I_d = 1\times10^{-7}$ A as indicated in Fig. 3. The loop was drawn in the counterclockwise direction. Figure 4 showed the retention characteristics where the two curves were corresponding to the programmed and the erased states. Before starting the hold, V_g = 6 V for the programmed and V_g = -4 V for the erased were applied for 100 ms individually. The hold voltage was V_g = 0.8 V during the measurements. Good retention was obtained which kept a large 10^5 I_d ratio even at 3.98×10^5 s between the erased and the programmed curves. High endurance of 10^8 cycles was also obtained as shown in Figs. 5. The endurance pulses were repeated $V_g = \pm 6$ V with 20 μs period. The reference I_d for judging the V_{th} was $I_d = 1\times10^{-7}$ A. The FeFET showed very stable endurance keeping 1.0 V V_{th} difference even after 10^8 cycle measurements.

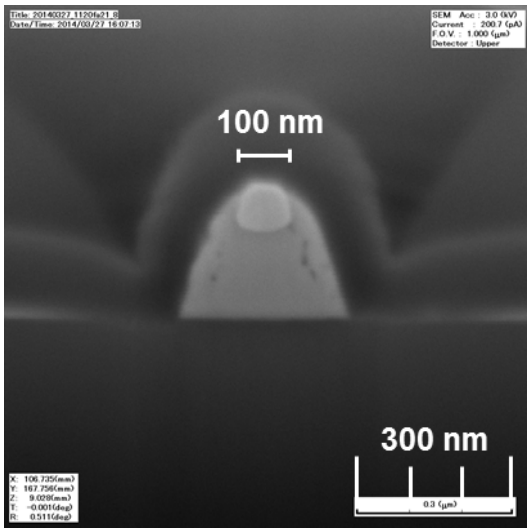

Fig. 2 Cross sectional photo of FeFET obtained by FIB-SEM.

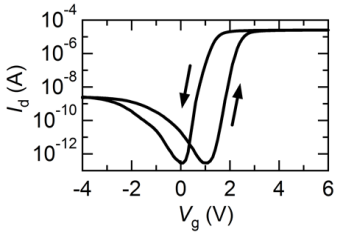

Fig. 3 I_d-V_g at V_g = 1±5 V of FeFET.

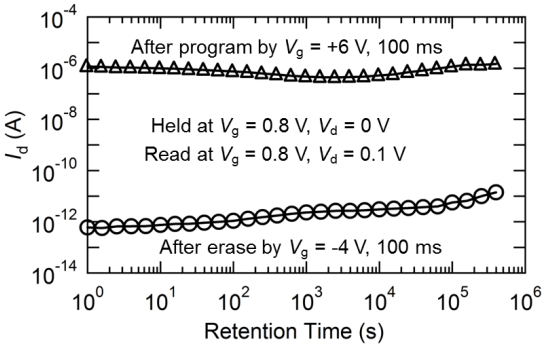

Fig. 4 I_d-retention of FeFET by applying V_g = +6 V for100 ms to program and V_g = -4 V for 100 ms to erase.

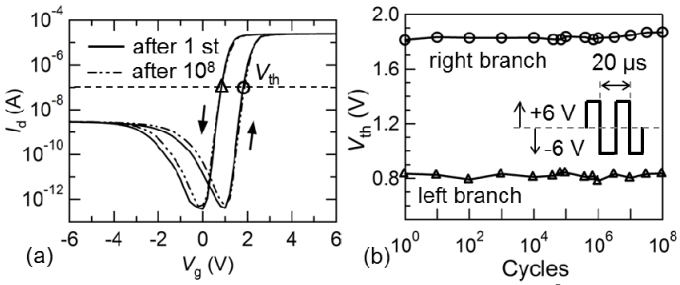

Fig. 5 (a) I_d-V_g at V_g = ±6 V of FeFET at the first and 10^8 cycles. (b) Endurance by applying 10^8 cycles of V_g = ±6 V with 20 μs period.

4. Conclusions

Downsized FeFETs with L = 100 nm were successfully produced by using SCBT for the core ferroelectric materials in the FeFETs, covering the sidewalls by SCBT films, and fine-etching by optimized conditions. The FeFETs showed wide memory windows about 1.1 V. They also had good electric properties such as long retention measured for about 4×10^5 s and high endurance counted up to 10^8 cycles.

Acknowledgements

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