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Back Gate Bias-Temperature Instability in Single-Layer Double-Gated Graphene Field-Effect Transistors

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Abstract

We study the bias-temperature instability (BTI) on the back gate of double-gated graphene field-effect transistors (GFETs). The dependence of the resulting degradation on the stress time and oxide field is analyzed. Finally, the results are compared to the ones obtained on the high-k top gate of the same device.

1. Introduction

Graphene is a superior 2D material [1-3] which is considered a promising candidate for various industrial applications. In particular, different groups have recently succeeded in fabricating graphene FETs (e.g. [4-6]). Nevertheless, there are only a few attempts to describe the reliability of GFETs [7-10]. Here we study the bias-temperature instability resulting from a voltage applied on the back gate of double-gated GFET. We show that there is an asymmetry between positive BTI (PBTI) and negative BTI (NBTI) in terms of the degradation magnitude and its dependence on the stress oxide field. Finally, we compare the results obtained on the SiO_2 back gate and higk-k top gate of the same device.

2. Devices

We perform our study on single-layer double-gated GFETs fabricated using a standard lithography process [11]. Contrary to our previous work [12], the thickness of the back gate SiO_2 in these devices is 92 nm (cf. 1800 nm in [12]), which allowed us to observe back gate BTI at reasonable stress voltages. The top gate insulator is 25 nm thick Al_2O_3, while the channel length is 4 µm and width 80 µm. Also, in order to reduce the device-to-device variability, the devices have been baked at T = 300°C for 5 hours before the experiments.

3. Experiment

All our experiments were performed in vacuum (~ 10^{-5} torr), in order to avoid the detrimental impact of the environment [10]. The BTI dynamics were examined as follows: after measuring the reference gate transfer characteristics, the subsequent stresses with increasing V_{BG}-V_D (back gate voltage minus Dirac point voltage) and top gate voltage V_{TG} = 0 were applied. The resulting gate transfer characteristics were measured after each stress, while in some cases the recovery of the stressed device was monitored as well. A similar technique with increasing V_{TG}-V_D and V_{BG} = 0 was applied for the top gate BTI measurements.

4. Results and Discussions

In Fig.1a we show the measured evolution of the back gate transfer characteristics after the subsequent NBTI and PBTI stresses. As suggested in [12], we express the degradation magnitude in terms of a Dirac point voltage shift ΔV_D. The resulting dependences of ΔV_D on the stress oxide field $F_{ox} = (V_{BG} - V_D)/d_{ox}$ are plotted in Fig.1b for two different stress times t_s. Contrary to Si technologies, in both cases PBTI degradation is stronger than NBTI and the dependences of their magnitudes on F_{ox} are different. While the NBTI shift linearly increases versus F_{ox}, growth of

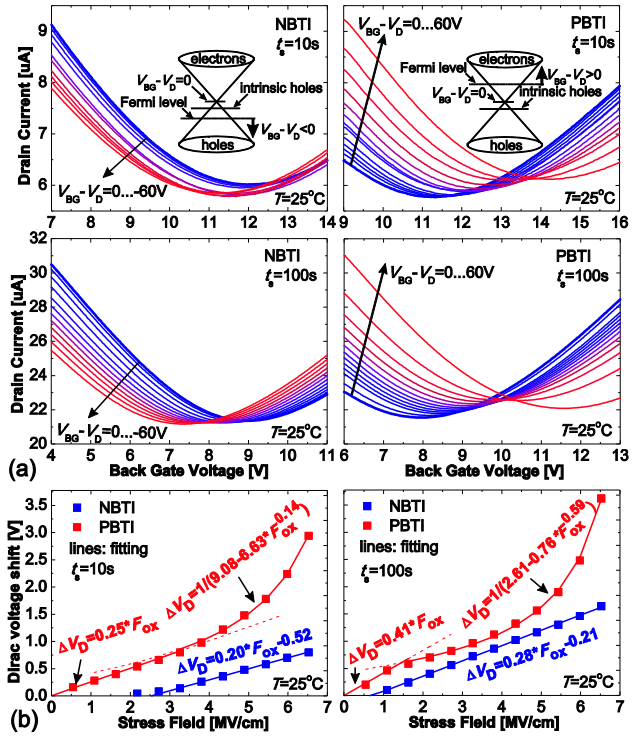

Fig.1. (a) Evolution of the back gate transfer characteristics after subsequent stresses with increasing V_{BG}-V_D and two different stress times for NBTI (left) and PBTI (right). (b) The resulting V_D shift versus stress oxide field for t_s=10s (left) and t_s=100s (right).

PBTI shift is linear only at small F_{ox} and can be fitted with a Langmuir power law $f(x)=1/(a-bx^c)$ at larger oxide fields. Interestingly, for both NBTI and PBTI the slopes in the linear regions increase versus t_s, since the probability of carrier trapping is larger for longer stresses. At the same time, transition of PBTI curves to a Langmuir-like behavior takes place at smaller F_{ox} if t_s is larger. This leads to a smaller difference between PBTI and NBTI shifts at moderate F_{ox} (Fig.1b, right). Since in GFETs PBTI is associated with electron trapping and NBTI with hole trapping, we assume that the main reason for the observed behavior is the difference in the kinetics of the two processes, as well as the energetic alignment of the defect bands with the

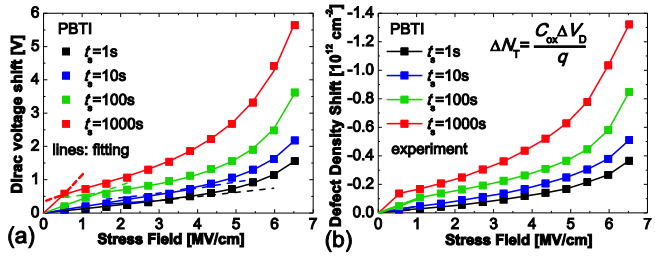

Fig.2. Stress field dependence of the ΔV_D (a) and ΔN_T (b) after PBTI stresses with different t_s. $\Delta N_T<0$ means electron trapping.

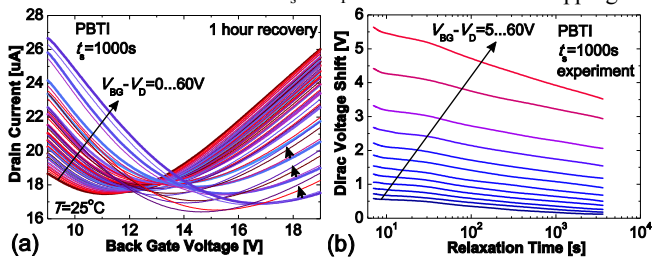

Fig.3. (a) Time evolution of the back gate transfer characteristics after subsequent PBTI stress/recovery rounds with increasing V_{BG}-V_D. (b) The corresponding ΔV_D recovery traces.

Fermi level in the graphene channel. Another issue which contributes to the asymmetry between NBTI and PBTI is the positive V_D, which means that our graphene is p-doped. Thus NBTI degradation is not pronounced at small F_{ox}, when the applied voltage is not enough to shift the Fermi level below the intrinsic level (Fig.1a, inset). As for PBTI, even after a stress with t_s=1s and F_{ox}<1MV/cm some degradation is clearly visible (Fig.2a). Interestingly, if the stress time is small, the PBTI shift moderately increases in a linear manner up to quite large F_{ox}. Conversely, in the case of long stresses a linear increase of ΔV_D is abrupt and observed only in a very narrow range of small F_{ox}, being immediately substituted by a Langmuir-like behavior. Obviously, the same type of oxide field dependence is typical for the defect density shift ΔN_T, which is proportional to ΔV_D (Fig.2b). However, the values of ΔN_T observed for GFETs are 10^{11}-10^{12} cm^{-2}, which is significantly larger than for Si technologies (10^{10} cm^{-2}). In Fig.3 we demonstrate that the back gate PBTI degradation in GFETs is recoverable, similarly to its counterpart observed on the high-k top gate [12]. The distances between the recovery traces increase for larger V_{BG}-V_D, following the Langmuir-like dependence which is typical for t_s=1000s (cf. Fig.2a). Finally, in Fig.4 we compare PBTI degradation on the SiO_2 back gate and Al_2O_3 top gate of the same GFET. Since the two oxides have a different thickness, we operate with $\Delta V_{Dn}=\Delta V_D/d_{ox}$. Clearly, the magnitude of PBTI degradation on the top gate is considerably larger (Fig.4c). This is similar to Si technologies, where the reliability of high-k oxides presents an important issue [13]. Also, the dependence on

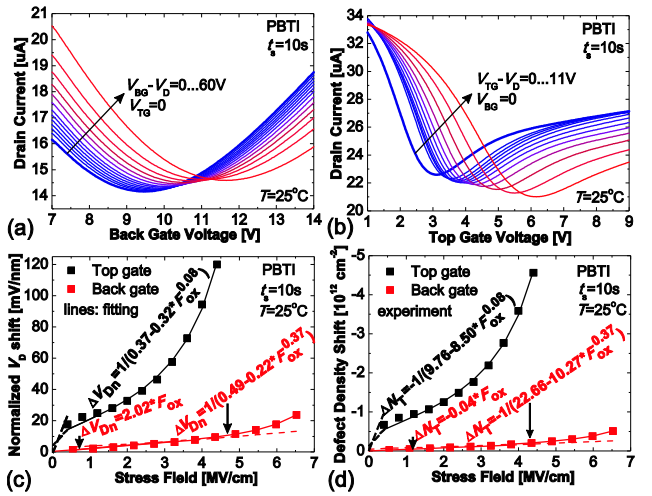

Fig.4. Evolution of the back gate (a) and top gate (b) transfer characteristics after the subsequent PBTI stresses with increasing oxide field. Comparison of the resulting ΔV_{Dn} (c) and ΔN_T (d).

F_{ox} in the case of top gate PBTI is purely Langmuir-like, while an abrupt linear increase is expected only close to F_{ox} =0, to maintain zero degradation at zero oxide field. This is despite t_s=10s, which leads to a significant linear region in the case of back gate PBTI. Obviously, the defect density shift is also larger for the top gate PBTI (Fig.4d).

5. Conclusions

We performed an experimental study of BTI on the back gate of double-gated GFETs. It has been found that there is a considerable asymmetry between NBTI and PBTI in terms of degradation magnitude and its dependence on the stress parameters. Finally, the degradation dynamics are similar to the one observed on the high-k top gate, although the magnitude in the latter case is significantly larger.

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