Extended Abstracts of the 2016 International Conference on Solid State Devices and Materials, Tsukuba, 2016, pp41-42

A-5-03

An Investigation of the Parasitic RC Effects in Nano-scaled FinFETs and Its Impact on SRAM Cells

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Abstract

As parasitic RC effect become more and more prominent in nano-scaled FinFET technologies, it is critical to the final overall circuit performance. In this study, the parasitic resistance and capacitance effect of a single-fin FinFET on standard logic CMOS devices and circuits process are investigated, respectively. In addition, effect of dummy patterns as well as multi-fin structures are analyzed and modeled in details. Incorporating the parasitic resistance and capacitance extracted by both measurement and simulation data, the static and dynamic performance of standard 6T-SRAMs is comprehensively evaluated.

Introduction

The presence of parasitic resistance and capacitance in a transistor is unavoidable. With the rapidly advancement in CMOS technologies, scaling well into the sub-20nm regime, multi-gate structures, such as FinFET, becomes the mainstream technology. The mitigation from planar to 3D transistor requires drastics change in its structure, such as, raised source/drain, fully depletion fin and high aspect ratio metal gates. These structure changes enhance parasitic effects, which in turn, degrades the overall device and circuit performance, subsequently. The impact of parasitic resistance and capacitance on the overall device performance are become more prominent as technology scaled[1]. To fascilitate the forming of fine pattern in such advance technologies, dummy patterns are added in the circuit layout design, which has become anecessity to reduce loading and edge effects during fabrication process. These dummy patterns can further increase the parasitic effect on the transistors and thereby subsequently circuits.The increase of parasitic resistance and capacitance from the transistor may have negative influence various aspect of the circuit performance[2-3] . In this work,a standard model of the parasitic RC for a single-fin FinFET is constructed and expanded to multiple-fin FinFET structure. Lastly, the impact of parasitic effects in circuit is demonstrated in standard 6T-SRAM as well.

Parasitic RC in Single-fin FinFETs

The 3-Dimensional (3D) schematic of the FinFET structure is illustrated in Figure 1(a). The cross-sectional TEM picture of a FinFET with raised epitaxial source/drain is shown in Figure 1(b). The various components contributing to the overall parasitic resistance is outlined in Figure 2(a), which includes Lightly-doped drain (LDD) resistance(R_{EXT}), contact resistance (R_C), and source drain resistance(R_{SD}). Through comprehensive extraction method in our previous work [4], ratio of each components can be found, as shown in Figure 2(b). The overall parasitic resistance(R_P) in a single fin FinFET can take up over 30% of the overall resistance of a fully turn-on transistor. Top-view of a single-fin FinFET is shown in Figure 3(a), where Figure 3(b) indicates parasitic capacitance elements along AA' cross-section and Figure 3(c) indicates parasitic capacitance components from BB' cross-section. Total capacitance, C_T, in FinFET includes, oxide capacitance (C_{OX}), Epitaxy capacitance (C_{EPI}), shallow trench isolation (STI) capacitance (C_{STI}), and contact capacitance (C_{CO}). The ratio of each components obtained measurement and simulation data are summarized in Figure 3(d). To extract the parasitic capacitance(R_P) and capacitance(C_P), a 3D single-fin FinFET structure is defined in TCAD simulator. Figure 4(a) and (b) demonstrate the simulated CV characteristics and I_DV_G characteristics, which agree very well with measurement data.

Multi-Fin Transistor and Dummy Patterns

Transistor width in FinFET are increased by adding number of fins in a device. In multi-fin structure, parasitic RC effects changes, accordingly. R_P and C_P in FinFETs with 2 or 4 fins are simulated. The 3D schematic of 4 fins FinFET is shown in inset of Figure 5. The R_P extracted by channel modulaiton method at low drain of 50mV is compared in Figure 5.Figure 6 summarized the CV characteristics of multi-fin transistors. Data in Figure 5 and Figure 6 indicates that both C_P and R_P are proportional to number of fin. The ratio between channel resistance and parasitic resistance and that between oxide capacitance and parasitic capacitance in transistor with different number of fin are summarized in Figure 7. In read circuits, a transistor is seldom placed alone, but rather often densely packed. To enhance the yield rate of product, dummy patterns is often added deliberately to ensure even pattern density. In this investigate, dummy gates are added on the both side of the transistor's metal gate. The 3D schematic of simulation structure is shown in the inset of Figure8. The comparison of total parasitic resistance with or without additional dummy gates under different numbers of fin suggests that the adjacent dummy gates does slightly enhance the parasitic capacitance.

Parasitic RC Effect on 6T SRAM

Parasitic effects can futher affect to overall circuit performance. A conventional 6T SRAM [5-6] are employed as the example for benchmarking RC effect. Figure 9 shows the layout of a standard 6T SRAM cell used in the following analysis. Dummy patterns are added for pattern density optimization. For SRAM, Static Noise Margin(SNM) in different operation modes and dynamic read stability time are generally regards as the key performance factors. R_P can be the cause of SNM degradation. Figure 10 compares the butterfly curves of SNM under read operations, using FinFETs with and without R_P. Figure 11 then compares the butterfly curves of SNM in write condition, using FinFETs with and without R_P. Dynamic response of a SRAM cell on the other hand will subject to effect of C_P more prominently. Here, dynamic read settling time of node Q and QB are evaluated for cells composed of FinFETs with or without parasitic effects. The parasitic effects induced by adding dummy gates are also compared by the transient response characteristics in Figure 12. Table 1 is the summary of SRAM performance factor with and without the parasitic effects. R_P causes seeable affect for both read and write conditions. Dummy gates cause minimal increase on parasitic capacitance. As a result, the dynamic read settling time are more significant affected by the introduction of C_P.

Conclusions

The parasitic resistance and capacitance model for a standard single-fin FinFET is established and expended to multi-fin FinFET structure. Effect of dummy patterns on parasitic RC are included. Finally,the parasitic RC effect of a FinFETs benchmarked evaluating the static state and dynamic performance of a 6T SRAM example.

Acknowledgement

This research was supported in part by the Ministry of Science and Technology, Taiwan, and in part by Taiwan Semiconductor Manufacturing Company.

References

[1] A. N. Bhoj, et al. TVLSI, Vol. 21, No. 11, p. 2094, 2013

[2] D. Bhattacharya, et al. TVLSI, Vol. 24, No.1, p. 329, 2016

[3]J. J. Kim, et al. EDL, Vol. 30, No. 8, p. 852, 2009

[4] F. H. Meng, et al. JJAP, Vol. 55, No. 4, p. 04ED16,2016

[5] C. C. Wu, et al. IEDM, p. 27.1.1 , 2010

[6]S. Y. Chien, et al. TED, Vol. 61, No. 11, p. 3731, 2014

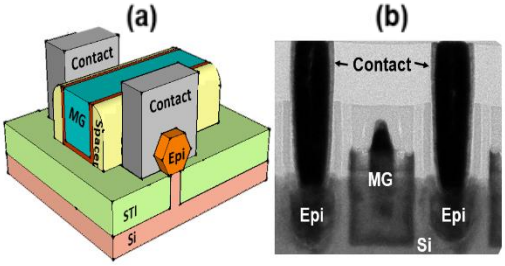


Figure 1 (a) A 3D illustration of the standard 16nm single-fin FinFETs, and the cross-sectional TEM of a standard 16nm single-fin FinFET investigated in this work.

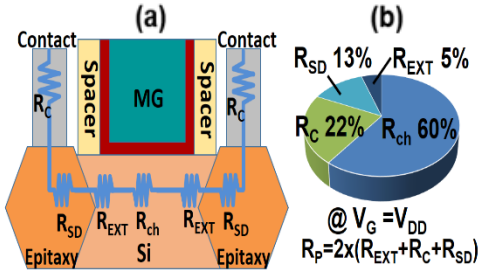
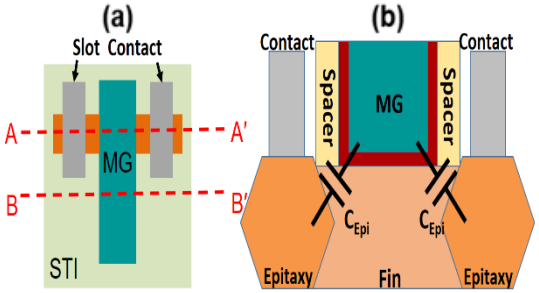


Figure 2 (a)The cross-section illustration of a single-fin FinFET. (b) The total resistance is broken down into four main components.



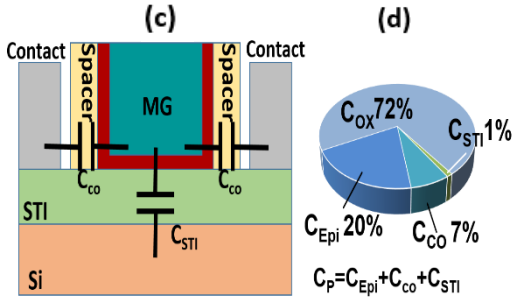


Figure 3 (a) Top view of a single-fin FinFET. (b) AA′ cross-section area with parasitic capacitance model. (c) BB′ cross-section area with parasitic capacitance model. (d) The total capacitance is composed of five major components.

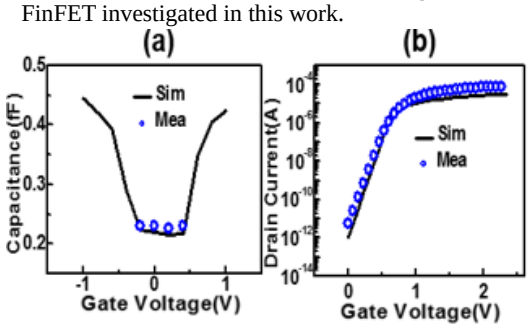


Figure 4 (a) Simulated CV characteristic and parasitic capacitance (C_P) measurement results. (b) Simulated and measured I_DV_G curves.

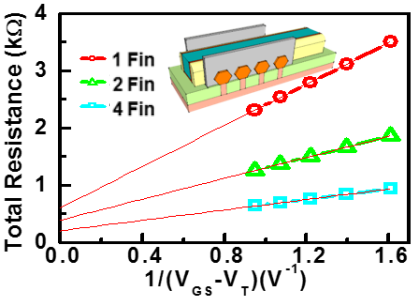


Figure 5 Simulation results of multi-fin FinFET parasitic resistance (R_P) extraction with channel modulaiton method at low drain of 50mV.

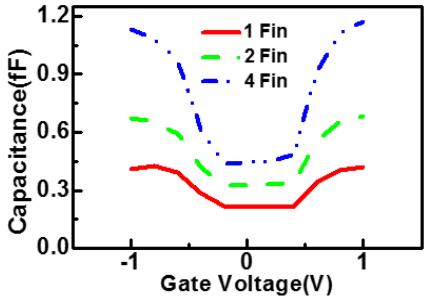


Figure 6 Simulation CV characteristics of the multi-fin FinFETs, including its various parasitic components outlines in Figure 3.

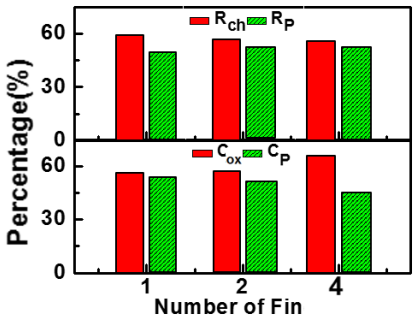


Figure 7 Extracted parasitic RC of multi-fin FinFETs as compared to the corresponding channel resistance and gate capacitance.

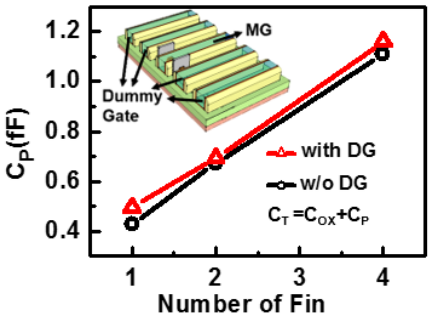


Figure 8 Simulation results show that adding dummy gate(DG) lead to slight increase in overall parasitic capacitance levels.

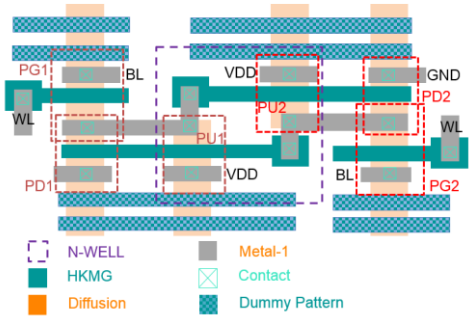


Figure 9 Layout illustration of a conventional 6T SRAM cell with dummy pattern, i.e. dummy gates for edge protections.

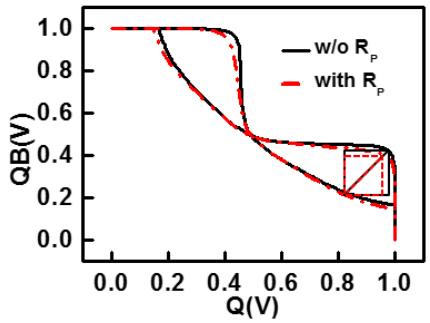


Figure 10 Comparison of read SNMs with and without R_P in FinFETs, reveals some degradation resulting from the parasitic resistance effects.

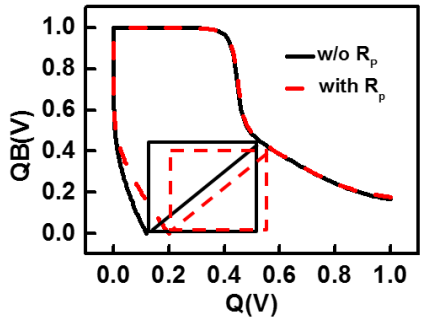


Figure 11 Comparison of SNM in write condition with and without R_P reveal some degradation at the presence of parasitic resistance effects.

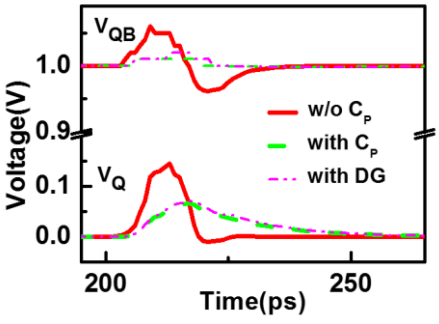


Figure12 Dynamic read settling responses of 6T SRAM with and without C_P and that with dummy gates.

		RSNM (mV)	WSNM (mV)
(a)	w/o R_P	179	401
	with R_P	143	341

		Settling Time (ps)	
		Q	QB
(b)	w/o C_P	32	31
	with C_P	26	49
	with DG	17	51

Table 1 Summary of SRAM static and dynamic performance under effect of parasitic resistance and capacitance. Data suggests that significant degradation can occurred in dynamic operations.