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# Key advanced technology for eMRAM development

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**Abstract**

Spin transfer torque magnetic random access memory (STT-MRAM) is one of most promising among new memory candidates. Our STT-MRAM technology is very close to the point of mass production. Application targeting is replacing embedded non-volatile memory (eNVM) at 28nm technology node. MTJ short fail development, Retention, endurance reliability improvement and write fail reducing technology have played key roles to develop eMRAM ready for mass production stage.

## 1. Introduction

For several decades, the development of memory industry was quite successful, doubling capacity for every two years. In the meantime, incumbent memories like SRAM, DRAM and Flash memories have their own strengths and area in the memory hierarchy system. So they are not easily replaceable by other memories. However, for a new era of Internet-Of-Things (IOT) and wearable devices open new opportunities for new memories. For example reducing power becomes more important than ever before. Among many new memory candidates, STT-MRAM is very attracting due to its fast read/write speed, non-volatility and practically unlimited read, write endurance. Thanks to several years' development, we are close to the point of STT-MRAM mass production at 28nm logic process[1]. In this presentation, focus will be advanced development of MRAM technologies which enables STT-MRAM obtaining technical maturity from a mass production perspective.

## 2. eMRAM development

Vertical TEM picture of MRAM cell array is illustrated in Fig. 1. MTJ (Magnetic Tunnel Junction) module inserted between 28nm Cu BEOL layers consists of MTJ stack and bottom electrode contact (BEC).

MTJ short fail is one of most critical technological hurdles to realize MRAM technology as a mass production level. Patterning metallic layers without deteriorating MTJ magnetic and electrical properties requires highly advanced patterning technology, considering very thin MgO insulating barrier. To avoid MTJ degradation, ion beam etching (IBE) process was employed for MTJ patterning. By adjusting parameters such as power, angle, etching sequences, we were able to reach MTJ short fail below 1ppm level as shown in Fig. 2.

Other than short fail, reducing parametric fail is crucial to obtaining good enough yields for commercialization of eMRAM. To minimize read fail, Tunnel Magneto Resistance (TMR) and MTJ resistance variation needs to be improved. Write fail is in a tradeoff relation with retention reliability. Reducing write fail while keeping retention reliability same requires MTJ stack improvement.

Reliability is also a key aspect for the commercialization of new memory. One of strength of MRAM is that there's no degradation of resistance distribution happens after endurance cycling. Parallel state (P-state) resistance distributions of MRAM from initial state to after 30M endurance cycle are shown in Fig. 3.

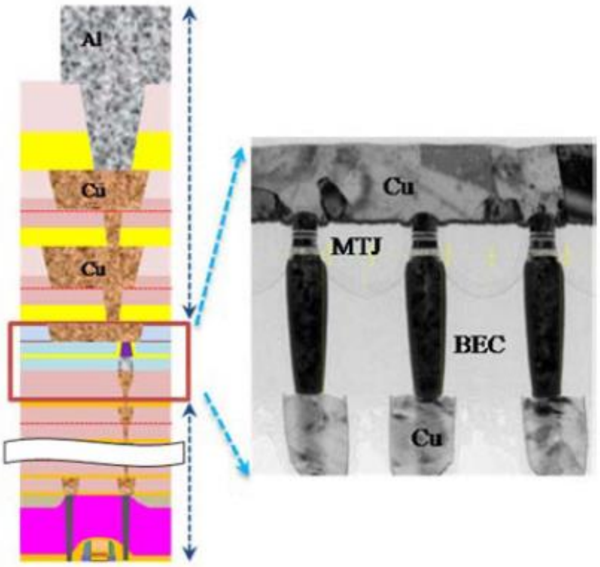


Fig. 1 Vertical structure of 8Mb STT-MRAM cell embedded in 28nm logic process..

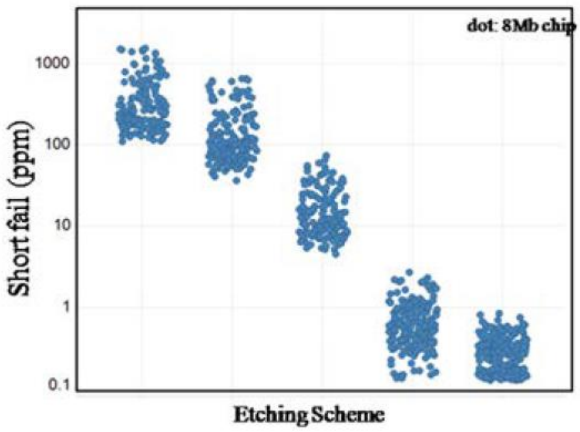


Fig. 2 Short fail trend of 8Mb macro for different etching conditions. It has been decreased below 1 ppm level by modifying ion beam etching condtions.

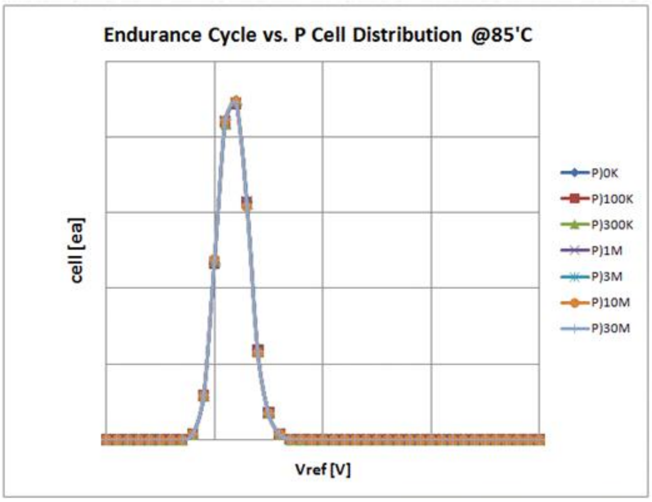


Fig. 3. Resistance distribution before and after endurance cycling. No degradation of distribution has been detected up to 30M cycle.

**3. Conclusions**

Key technology for eMRAM development will be introduced in this presentation including from hard fail, parametric fail improvement to reliability issues such as retention and endurance. Feasibility of mass production of eMRAM at 28nm node and beyond would be discussed.

**References**

[1] Y. J. Song *et al.*, “Highly functional and reliable 8Mb STT-MRAM embedded in 28nm logic” in Proc. IEEE *International Electron Devices Meeting, Dec. 2016, pp. 27.2.1-27.2.4*