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(Invited) GeSn/GeSi Stacked Channel Transistors

Chien-Te Tu, Bo-Wei Huang, Chung-En Tsai, Yi-Chun Liu, and C. W. Liu*

Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.
* E-mail: cliu@ntu.edu.tw

Abstract

4-stacked undoped $Ge_{0.9}Sn_{0.1}$ nanosheets sandwiched by double $Ge_{0.95}Sn_{0.05}$ caps without parasitic Ge channels are realized by radical-based highly selective isotropic dry etching, and 2-stacked $Ge_{0.98}Si_{0.02}$ nanowires without parasitic Ge and Si channels are demonstrated by optimized etching process. Heavily doped Ge sacrificial layers and undoped GeSn/GeSi channel layers can reduce the S/D resistance and suppressed impurity scattering in the channels, respectively. High inter-channel uniformity of the 4-stacked $Ge_{0.9}Sn_{0.1}$ nanosheets and record I_{ON} of 73μA per stack at $V_{OV}=V_{DS}=-0.5V$ among GeSn 3D pFETs are achieved. The 2-stacked $Ge_{0.98}Si_{0.02}$ nanowires with Si incorporation as small as 2% into Ge can achieve sufficient etching selectivity for channel releasing, and the device achieves record I_{ON} of 48μA per stack at $V_{OV}=V_{DS}=0.5V$ and record $G_{m,max}$ of 136μS at $V_{DS}=0.5V$ among Ge 3D nFETs.

Introduction

Si FinFET CMOS has been used in the industry for several technology nodes. Recently, gate-all-around (GAA) structure has been demonstrated as a promising candidate to extend the scaling beyond FinFET limits [1]. Vertically stacked GAA channels can provide large I_{ON} for a fixed footprint to achieve high performance and area scaling for advanced technology node. The channel thickness of vertically stacked channels is defined by epitaxy rather than lithography, and can be precisely controlled. Although stacked Si channel n/pGAAFETs has been demonstrated [2-5], high mobility channel materials such as GeSn [6-10] and GeSi [11-12] are good candidate for further performance enhancement.

In this work, we demonstrate vertically stacked compressively strained GeSn channels for pFETs [8-9] and tensily strained GeSi channels for nFETs [11]. GeSn and GeSi channels are grown on strain-relaxed Ge buffer to obtain an epitaxial biaxial compressive strain and tensile strain, respectively. The Ge buffer and Ge sacrificial layers (SLs) grown by CVD not only used to provide stress for the effective mass reduction and mobility improvement, but also can be selectively etched over GeSi and GeSn channel layers to form the vertically stacked GAAFETs.

CVD Epitaxy and Device Fabrication

For both GeSn and GeSi epi structure, the top Si of a 200mm SOI substrate was thinned down from 70 to 20nm by oxidation and buffered oxide etch. The thick and undoped Ge buffer was grown on SOI wafer by RTCVD with an additional *in-situ* annealing at 800°C. The anneal after the Ge buffer growth further improve the epi quality by confining misfit dislocations near the Ge/Si interface. For the epi structure of GeSn, B-doped Ge SL, $Ge_{0.95}Sn_{0.05}$ cap, $Ge_{0.9}Sn_{0.1}$ channel, and $Ge_{0.95}Sn_{0.05}$ cap were deposited repeatedly on Ge buffer using Ge_2H_6 and $SnCl_4$ as the precorsurs. The heavily B-doped ([B]~2E21cm^{-3} obtained by SIMS) Ge SLs are used to reduce the S/D resistance, and the undoped $Ge_{0.95}Sn_{0.05}$ caps and $Ge_{0.9}Sn_{0.1}$ channels are used to suppress the impurity scattering. The Ge buffers have ~0.15% tensile strain due to the mismatch of thermal expansion coefficients between Ge and Si. The $Ge_{0.95}Sn_{0.05}$ caps and $Ge_{0.9}Sn_{0.1}$ channels are fully compressively strained on Ge buffer with the strain of -0.59%, and -1.32%, respectively. The epitaxial biaxial compressive strain breaks the degeneracy of heavy-hole (HH) and light-hole (LH) bands of GeSn and leads to the rise of the LH band along the [110] transport direction [13-14]. Moreover, the effective mass of LHs at zone center is further reduced by the increasing compressive strain [15-16] for mobility enhancemnet.

For the epi structure of GeSi, the stacked $Ge_{0.98}Si_{0.02}$/Ge layers were grown on Ge buffer using SiH_4 and GeH_4 as precursors. The Ge buffer is 0.12% tensily strained after the 800°C annealing, and the $Ge_{0.98}Si_{0.02}$ channel layers have the 0.2% tensile strain. The 2% Si incorporated and fully strained GeSi channels are obtained by RSM. The heavily P-doped ([P]~2E20cm^{-3}) Ge SLs can reduce the S/D parasitic resistance, and the undoped channels can reduce the impurity scattering. The GeSi channels with only 2% Si can introduce the minimal alloy scattering and ensure the electrons populated in L valleys for small effective mass. The epi-layers quality for both GeSn and GeSi layers can be confirmed by the good photoluminescence which indicates sufficiently low point defect density.

After CVD epitaxy and SiO_2 hard mask deposition, the e-beam lithography and Cl_2-based RIE were used to form the fin structures. The RIE would result in GeSn layer side etching due to the weaker bond of Ge-Sn than Ge-Ge. Thin GeSn (5nm) channels can prevent the severe side etch by RIE to reach high inter-channel uniformity **(Fig. 1(a))**. On the contrary, severe side etch and the results of different channel width were observed for the thick GeSn (18nm) channels in our previous work [7] **(Fig. 1(b))**. After the field oxide definition, the channel release of GeSn channels was performed by highly selective isotropic dry etching (HiSIDE). HiSIDE system with NF_3 as process gas for the source to provide F radicals. The radical-based HiSIDE system can fully selective etch of Ge SLs and maintain GeSn channels. On the other hand, the channel release of GeSi channels was composed of three steps, in order to fully etch away parasitic channels. After fin formation, Cl_2/HBr RIE was used to form a reverse

tapered fin. Ultrasonic-assist TMAH etching at 60°C was then used to completely remove the Si underneath the Ge buffer. Finally, the Ge buffer and the Ge SLs in the channel region were completely etched by optimized ultrasonic-assist H_2O_2 to form the stacked $Ge_{0.98}Si_{0.02}$ nanowires with no parasitic channel **(Fig. 2)**. The etching selectivity of Ge over $Ge_{0.98}Si_{0.02}$ is attributed to the 2% Si in GeSi layer.

The gate stack of *in-situ* $TiN/ZrO_2/Al_2O_3/GeO_x$ was conformally formed around the channels by ALD and RTO. The following 400°C FGA was used to crystallize ZrO_2 for a large k value. Thick PVD layers of TiN was then deposited as the metal pads.

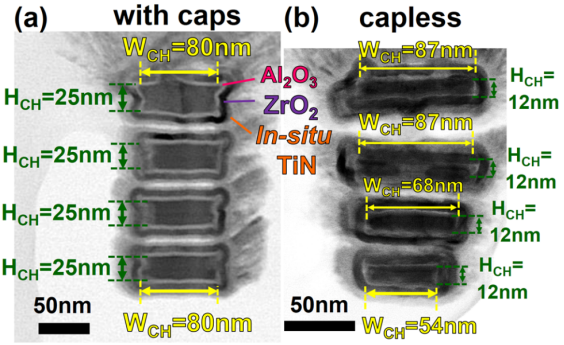

Fig. 1 (a) TEM image of the stacked four $Ge_{0.9}Sn_{0.1}$ nanosheets with double $Ge_{0.95}Sn_{0.05}$ caps with uniform W_{CH}. (b) TEM of the nonuniform stacked GeSn capless nanosheets in our previous work [7].

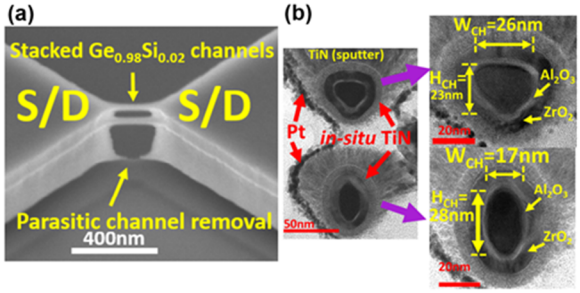

Fig. 2 (a) Tilt 52° SEM image of stacked $Ge_{0.98}Si_{0.02}$ channels. The parasitic channel is completely removed. (b) TEM images of the two stacked $Ge_{0.98}Si_{0.02}$ nanowires.

Device Performance

For stacked GeSn channels, the 4-stacked $Ge_{0.9}Sn_{0.1}$ nanosheets with thick double $Ge_{0.95}Sn_{0.05}$ caps are demonstrated to achieve uniform W_{CH} of 80nm due to the suppressed side etching by thin $Ge_{0.9}Sn_{0.1}$ channel and thick caps with low [Sn] during RIE, as compared to nonuniform channel width of the stacked GeSn nanosheets in our previous work. The decent SS of 105 mV/dec and record I_{ON} of 73μA per stack at V_{OV}=V_{DS}=-0.5V **(Fig. 3)** are achieved among GeSn 3D transistors due to the carrier separation from the dielectrics by caps, the low doping in channels, and the highly uniform W_{CH} among different channels.

For stacked GeSi channels, the $Ge_{0.98}Si_{0.02}$ layers are 0.2% tensily strained on Ge buffer, and lead to electron repopulation to L4 valleys with small transport mass and high mobility. The two stacked and tensily strained $Ge_{0.98}Si_{0.02}$ channels are fabricated with no parasitic channel to reduce leakage. The 2-stacked $Ge_{0.98}Si_{0.02}$ nanowires with scaled L_G = 40nm, record I_{ON} = 48 μA at V_{OV}=V_{DS}=0.5V, and record $G_{m,max}$ of 136 μS **(Fig. 4)** are achieved among 3D Ge nFETs and comparable to Si nFETs.

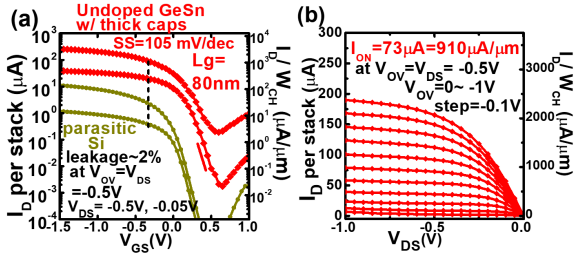

Fig. 3 (a) I_D-V_{GS} and (b) I_D-V_{DS} of the stacked 4 $Ge_{0.9}Sn_{0.1}$ nanosheets with double $Ge_{0.95}Sn_{0.05}$ caps.

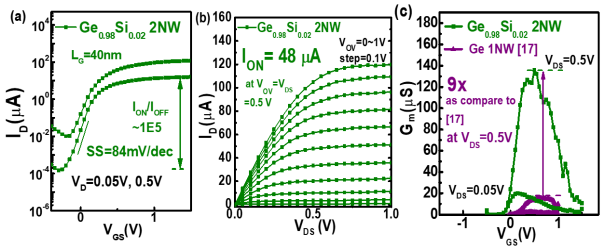

Fig. 4 (a) I_D-V_{GS}, (b) I_D-V_{DS}, and (c) G_m-V_{GS} of the stacked $Ge_{0.98}Si_{0.02}$ nanowires. $G_{m,max}$ is 9X higher than Ge nanowire of industry [17].

Conclusions

The double capped GeSn nanosheets with high interchannel W_{CH} uniformity and low channel doping are demonstrated to achieve high I_{ON} with novel HiSIDE system. Excellent electrical characteristics of GeSi nanowires are fabricated by simple wet etching.

Acknowledgements

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