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Co-integration of ReRAM with OTS back-end selector for high density Crosspoint arrays

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Abstract

This paper discusses the opportunity of 1S1R crosspoint arrays based on the integration of an HfO_2 ReRAM with OTS based selector. Guidelines are presented in order to accurately design the 1S1R stack and adjust the programming conditions in order to optimize device performances. Key device challenges such as scaling and variability are addressed.

1. Introduction

Our societies have entered in the big data era, characterized by an exponential growth of the amount of generated data (175ZB forecasted in 2025 [1]) and the explosion of the usage of connected objects in our everyday life. As digital technologies start having a significant impact on our carbon footprint [2], it is urgent to develop more energy saving systems and technologies. In this context, new architectures are required in order to improve computing system energy efficiency and reduce overall energy consumption. In particular, non-von-Neumann architectures are developed, including systems where part of the computation is made within the memory to limit the high power consumption linked to data transfer. This revolution offers huge opportunities for new technologies offering high capacity and low consumption. In particular, crosspoint architecture based on resistive memories (ReRAM) is one of the major candidate for current and emerging applications, including storage class memories [3] and future nodes embedded non-volatile memories. They would also constitute a significant breakthrough for neuromorphic circuits, and would open the path to analogue-hardware implementation of complex neuromorphic networks. Thus, they could significantly accelerate Deep Neural Networks for GPUs in high performance applications [4].

In this paper, we propose the developments of dense crosspoint arrays based on the co-integration of an Oxide ReRAM (OxRAM) with an OTS (Ovonic Threshold Switch) based back-end selector [5]. Technological challenges and key reliability aspects are presented and discussed.

2. Crosspoint technology

Device stack optimization

GeSeSbN (GSSN) was integrated as back-end OTS selector of HfO_2 based OxRAM memory in the BEOL of a 130nm CMOS process (**Fig.1**). GSSN offers good insulating properties, acceptable operating voltages and excellent endurance compatible with OxRAM properties [6]. GSSN thickness and composition optimization allow to control selector features [7]. Preventing material crystallization is one of the main OTS challenge and can be addressed by material engineering [8]. When designing the 1S1R stack, it is crucial to adjust the OxRAM and OTS thicknesses in order to control their switching voltages [9]. Indeed, when the OTS switches, most of the applied voltage drops on the OxRAM what can lead to memory degradation if the voltage is too high. **Fig.2** summarizes the optimized operating SET and RESET voltages as function of the OTS thickness, allowing to achieve high endurance 1S1R characteristics.

Scaling

Scaling the 1S1R structure results in variation of the device features. OxRAM bit error rate can increase of more than one order of magnitude as the cell size is scaled down to 30nm [10]. On the other hand, OTS characteristics are also impacted by scaling [11]. While switching, holding voltages and holding current remain constant, threshold and leakage currents scales with device area (**fig.4**). Thus, scaled OTS devices exhibit improved insulating capabilities with no counterpart in terms of switching voltage, suitable for high density crossbar integration.

Variability

Variability is one of the key challenge of 1S1R structures. OxRAM resistance dispersion (in particular in the High Resistive State) leads to a spread of 1S1R switching voltage (**fig.5**), which results in a narrowing of the read voltage margin. OTS switching voltage dispersion also contributes to device variability, and can be described by the dispersion of nucleation barrier in the field-induced nucleation theory [9].

Design

Adding a back-end selector in series to the OxRAM increases the device operating voltage, what may require the integration of high voltage transistor in the periphery. Assuming one driver transistor per bitline and per wordline, periphery contribution decreases as crossbar capacity increases (**fig.6**). Periphery can be accommodated below the memory crossbar arrays for tile sizes larger than tens of kb [12].

3. Conclusions

The potential of GSSN/HfO_2 1S1R stacks was discussed for crosspoint implementation. Reliability optimization were addressed based on experimental and theoretical investigations of 1S1R devices.

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References

[1] K. Ishimaru, IEEE IEDM 2019 Tech. Dig., pp.1.3.1-1.3.4.
[2] https://data-economy.com/data-centres-world-will-consume-1-5-earths-power-2025/
[3] K. Pangal, in IEEE IEDM 2017 Shortcourse.
[4] G. Burr et al., Advances in Physics, X, 2:1 (2017), pp.89-124.
[5] G. Molas et al., Proc. of 2020 IEEE Int. Mem. Workshop (IMW), pp.1-4.
[6] D. Alfaro Robayo et al., 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 35.3.1-35.3.4.
[7] D. Alfaro Robayo et al., Proc. of 2019 IEEE Int. Mem. Workshop (IMW), pp.1-4.
[8] C. Laguna et al., Proc. of 2021 IEEE Int. Mem. Workshop (IMW), pp.1-4.
[9] J. Minguet Lopez et al., 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, pp. 1-6.
[10] C. Cagli et al., 2019 IEEE International Electron Devices Meeting (IEDM), 2019, pp. 30.5.1-30.5.4.
[11] J. Minguet Lopez et al., Proc. of 2021 IEEE Int. Mem. Workshop (IMW), pp.1-4.
[12] J. Minguet Lopez et al., Proc. of 2020 IEEE Int. Mem. Workshop (IMW), pp.1-4.

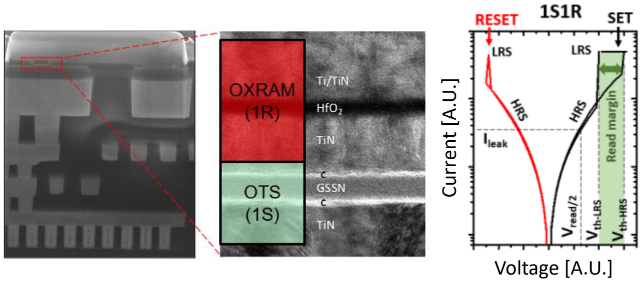

Fig.1 – SEM and TEM cross sections of the 1S1R device integrated in the BEOL over 130nm CMOS transistor. Right: typical 1S1R IV switching characteristics.

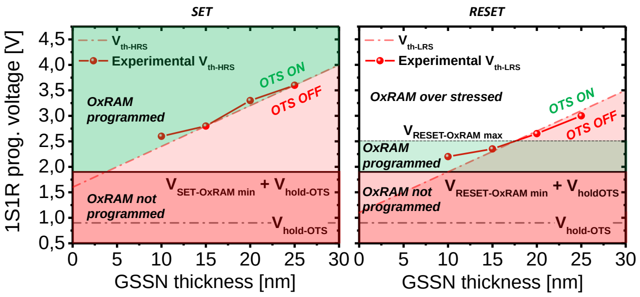

Fig.2 – 1S1R simulated and experimental switching voltage (V_{th-HRS} and V_{th-LRS}) during SET and RESET. Functional operating regions are highlighted where sufficient voltage is provided to both open the OTS and program the OxRAM.

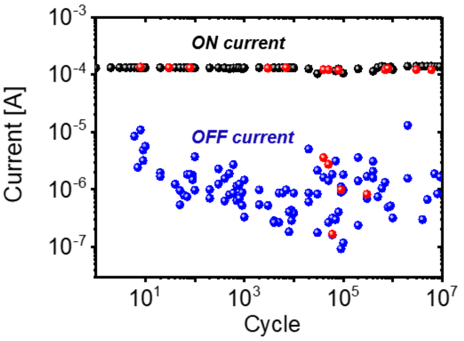

Fig.3 – 1S1R endurance obtained with optimized stack (15nm GSSN) and optimized programming conditions from fig.2.

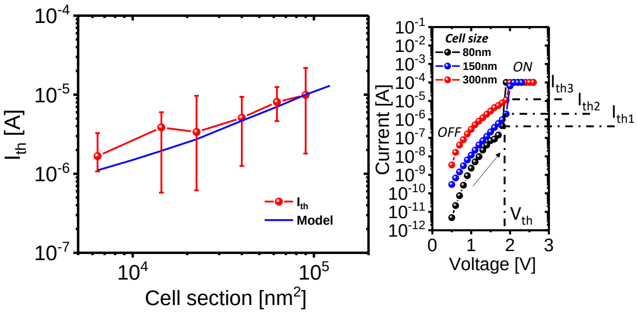

Fig.4 – Evolution of the GSSN OTS threshold current I_{th} with cell scaling. Model according to [9].

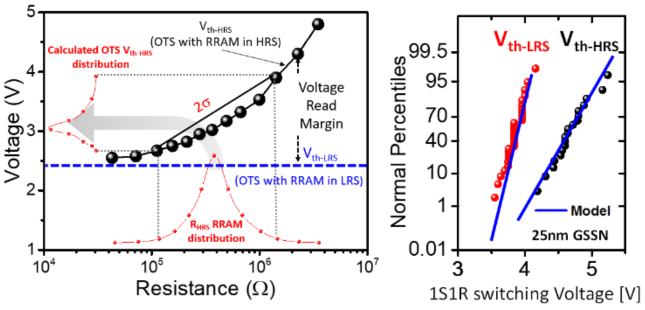

Fig.5 – Left: calculated 1S1R V_{th-HRS} as function of RRAM R_{HRS}. 1S1R voltage read margin is indicated. Right: measured and simulated 1S1R V_{th-HRS} and V_{th-LRS} distributions.

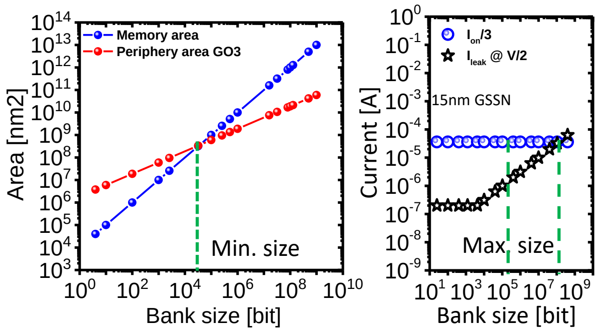

Fig.6 – Left: memory and periphery areas for 1S1R crosspoint as function of crosspoint size. Right: 1S1R cell read current compared to total crosspoint leakage current as function of crosspoint size.