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Booming Architecture and Device Innovations for Intelligent Semiconductor Era

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Compared with conventional "scaled" semiconductor, which is computation heavy and high-performance application driven, the intelligent semiconductor era has two features: 1) fusion of computation, memory and sensing; 2) smart application driven. This talk will discuss this topic with the concept of the "intelligent semiconductor tree", as shown in Fig. 1, which is an ecosystem tree with adaptive energy pipelines to deliver the computing power.

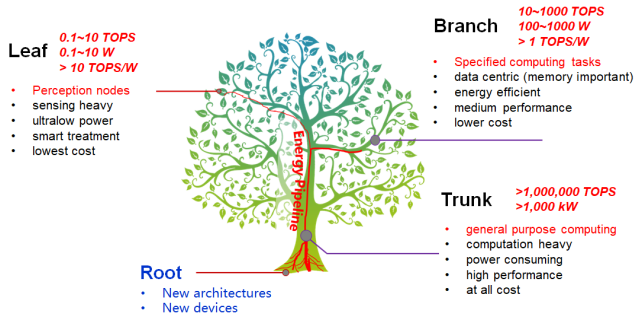

Fig. 1 The "intelligent semiconductor tree", from the perspective of computing power distribution.

With the intelligent semiconductor tree, not only the computing power distribution becomes more efficient, but also the data flow needs more intelligent design. This talk will focus on the recent root innovations from both new architectures and new devices for branch and leaf.

For the architecture innovations, the recent advances in near/in- memory computing (for the fusion of computation & memory) and near-sensor computing (for fusion of computation & sensing) will be presented. 1) For near/in-memory computing, a quick overview, state-of-the-art comparisons (capacity, energy efficiency, throughput, power, compute density, etc.) and some recent progress will be given. 2) For near-sensor computing, recent solutions of event-driven architecture and AI-earliest architecture (with ANN engine for static events, and SNN engine for dynamic events) will be discussed.

From device perspectives, the above new architectures actually expect new device innovations for further improvements: 1) In-memory computing architecture still needs low-cost energy-efficient memory devices, 2) Event-driven architecture needs ultralow-leakage low-cost logic device for always-on module, 3) AI-earliest architecture needs area-efficient artificial neurons for SNN engine.

Recent device innovations from the above three perspectives will be further discussed. 1) For low-cost energy-efficient memory, our work on ferroelectric transistor (FeFET) and BEOL-compatible 2T0C DRAM will be given; 2) For ultralow-leakage low-cost logic device, Si steep-slope FET technology platform, and BEOL-compatible FET with high conductive amorphous oxide semiconductor (AOS) channel will be presented; 3) For area-efficient artificial neurons, our work on FeFET-based advanced neuronal functions with compact hardware designs will be shown.

Two outlooks will be discussed finally: 1) the technology FoM and industrial logic is changing; 2) further expected research directions. As shown in Fig. 2, current research activities are focused on the energy efficiency and complexity (including integration complexity and architecture complexity). Apart from what have been presented above, two other research directions on complexity are emerged: function complexity in one device (e.g., all-in-one device) and physics complexity (e.g., nonlinear dynamics). Besides, the third dimension for future semiconductor, which is the fault tolerance, should also be paid more attention in the research community.

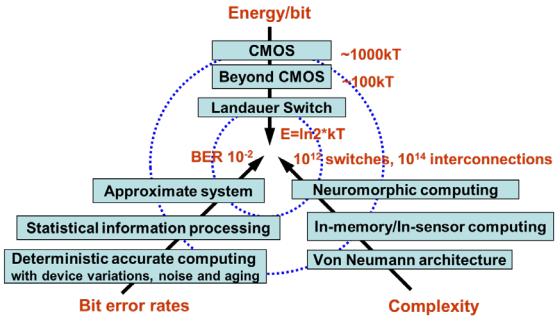

Fig. 2 Three research directions for intelligent semiconductors: energy efficiency, complexity, and fault tolerance.