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Cryogenic inter-chip connection for silicon qubit devices

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Abstract

Spin qubits in silicon quantum dots (QDs) are promising for realization of large-scale qubit systems, thanks to their scalability [1]. However, there are challenges to be overcome for the realization, such as problems on the interface between the qubit chip and peripheral control circuitry. Interposers are expected to serve as a viable solution for the interface for silicon qubits. In this paper, we report DC and RF characterizations of QDs on interposers at cryogenic temperatures. The results show the possibility of cryogenic interposer integration of spin qubit and peripheral control circuitry.

1. Introduction

It is considered that millions of qubits are required to realize a practical quantum computer. Silicon spin qubits are one of the favorable platforms because of compatibility with existing CMOS technology and a small qubit footprint. Nonetheless, interface between the qubit chip and peripheral control circuitry (Fig.1) [1,2] is a serious engineering challenge toward large-scale integration.

Using interposers is a promising route to evade the need for full single-chip integration of all functionalities. A warranted concern when transferring this established technology at room temperature to silicon qubit experiments is thermal stability down to cryogenic temperatures. In this paper, we report measurements of quantum dots (QDs) on a silicon interposer in liquid helium. We employ the electro-static discharge (ESD) protection circuit as a simple basic peripheral circuit. We flip-chip bond the QD chip and the ESD protection chips onto the silicon interposer and evaluate the DC and RF performance. In addition, we compare the QD characteristics before and after we laser cut the connection between the QD chip and the ESD chips on the interposer.

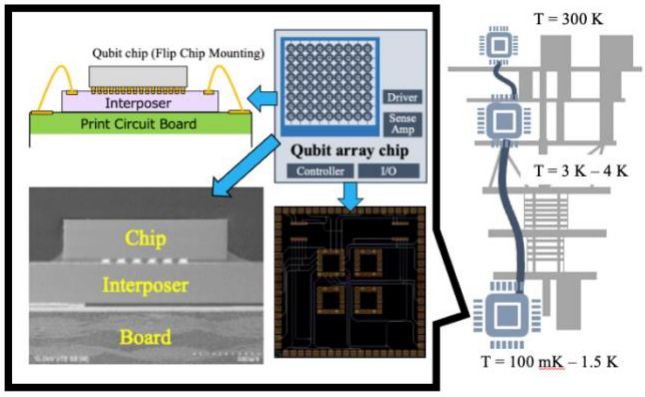

Fig. 1 Schematic picture of future integration of silicon qubits.

2. Structure of interposer

A silicon interposer allows much finer wiring patterns than a printed circuit board thanks to an advanced semiconductor manufacturing process. This enables to form high density pads and lead-outs for flip-chip implementation of future large-scale qubit chips with massive number of I/Os. The silicon interposer in this work is composed of two layers of Al metals with the width, space, and thickness of 7.5 μm, 7.5 μm, and 2 μm, respectively (Fig.1). The size of the interposer is 4 mm × 4 mm, and the qubit chip is flip-chip mounted in the middle of interposer through Au stud bumps. In addition to pitch conversion function for the qubit chip, this interposer also serves as a common substrate on which to mount other functional chips. This work demonstrates the implementation of two extra chips including ESD diodes to protect the qubit gate terminals from surges during wire bonding.

3. DC measurement

We first performed electrical characterization of the device on the interposer in liquid helium. Our aim is to confirm the electrical connection between the interposer and the qubit chip after thermal contraction by measuring quantum phenomena at cryogenic temperature.

Figure 2 shows Coulomb peaks and Coulomb diamonds, which were successfully measured using the silicon interposer at cryogenic temperature. We further confirmed that even after taking the device in and out of liquid helium a few times we were able to perform measurements without any problems.

4. RF measurement

For semiconductor-based spin qubits, fast pulses are used for control and readout, and hence, RF characteristics are also important. Employing flip-chip bonding for device connection may also help reduce RF crosstalk [3]. Here we focus on the technique called RF-reflectometry, which is often employed for fast readout [4]. A circuit diagram is shown in Fig. 3(a). Changes in the conductance and/or capacitance of the quantum dots can be read out using a resonance circuit comprising the inductance of a coil and the

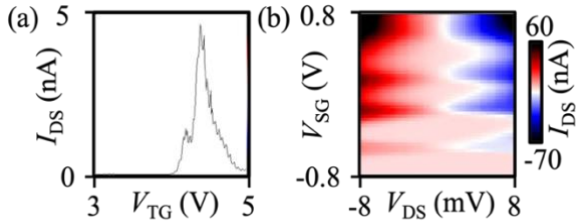

Fig. 2 The results of the QD measurement: (a) Coulomb peaks (b) Coulomb diamonds.

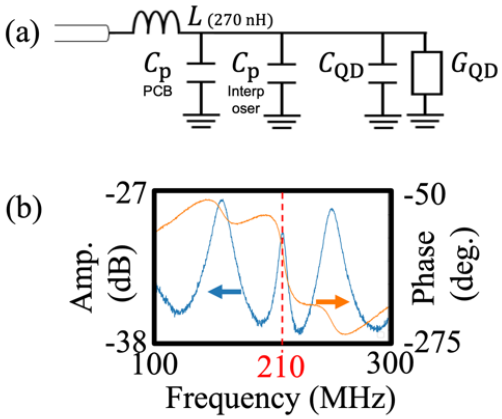

Fig. 3 (a) LC resonance circuit schematic used in this experiment. (b) RF characteristics of the LC circuit when the RF tone is applied to the drain of the QD.

parasitic capacitance(s). Assuming a (typical) total parasitic capacitance of our quantum dots device and print circuit board (PCB) of less than 1 pF [4] and an inductance of 270 nH, we expect a resonance frequency of about 400 MHz. However, the reflected phase and amplitude plotted in Fig.3(b) shows a resonance frequency of around 210 MHz, corresponding to a total parasitic capacitance of 2.9 pF. Such large capacitance is not desirable for RF-reflectometry because it reduces the sensitivity of the measurement [4]. Based on the characterization results of our first-generation silicon interposer chip, we envisage several possible scenarios to reduce the capacitance due to the interposer. Bond wires on the silicon interposer can be made shorter. Interposer layer structure can be revised with care taken for parasitic capacitance. With these improvements, we anticipate that the capacitance can be reduced to a level required for sensitive RF reflectometry.

5. Laser cut

In the experiment described above, we implement ESD chips in addition to the QD chip on the interposer. Since the ESD chips contain parasitic capacitive loads that may degrade the signal integrity of high-frequency pulses for future qubit control, we consider the possibility of cutting connections between the QD chip and unnecessary ESD chips just before measurements [5]. One of the methods to cut such connections is laser heating which has been used to cut metal wiring. This allows the QD measurements without the parasitic components of the ESD chips. However, the heat may cause damage to the device. Here, to know the impact of the laser on the QD, we compare the measurement result before and after a laser cut.

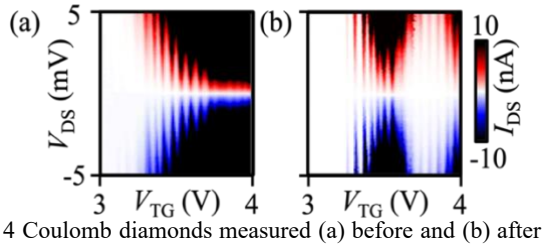

Fig. 4 Coulomb diamonds measured (a) before and (b) after a laser cut.

Figure 4 shows the measurement results before and after a laser cut. The wavelength and energy of the laser used in this experiment are 532 nm and 4 mJ/pulse, respectively. After the laser-cut, the QD is still working while the characteristics are measurably changed. The cause of changes in characteristics is not known yet: possible reasons include, besides damage caused by laser cut, impact of the device transportation and thermal cycle of the device. The fact that the QD works even after a laser cut is nevertheless a very positive result. We anticipate that in the future it is possible to put various chips on a silicon interposer and post-select only those necessary to measure qubits by the laser-cut technique.

6. Conclusions

In this paper, we tested the performance of silicon interposers. We demonstrated that the QDs can be electrically controlled and measured via the interposer at cryogenic temperature. Moreover, we cut the electrical connection between the QD electrodes and ESD protection chips by using laser heating, and observed the QD behaviors afterwards with changes in the characteristics. Future works include reducing parasitic capacitance for better RF performance, analyzing the cause of device characteristics change and need to improve structure, and integrating more functionalities with a qubit chip using the technique demonstrated in this work.

Acknowledgements

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