

Assessment and optimization of the cascaded transistor method for the direct extraction of access resistance components in FinFET and NSFET devices.

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Abstract

In this work, we have built calibrated TCAD decks for FinFET and NSFET devices, respectively, to validate our access resistance extraction method based on cascaded transistor test-structures. Besides the validation of the approach, we also propose an improved measurement set-up. Finally, we present some initial results from n-NSFET devices with 45 nm contacted poly pitch and 20 nm gate length, analyzing the impact of spike annealing steps.

1. Introduction

The continuous downscaling of logic MOSFET devices has put a great emphasis on the need to reduce the access resistance (R_{access}) components to maintain good ON-current performance as analyzed in many publications in recent years [1-3]. The R_{access} is typically composed of all resistive components that are not gate-controlled, namely the contact resistance (R_{cont}), the source/drain (S/D) epi resistance (R_{epi}) and, possibly, an additional interface resistance (R_{int}) component (when a heterojunction is present between S/D and channel) [4-5]. As we progressively move from FinFET towards nanosheetFET (NSFET) technologies with further reduced contacted poly pitch (CPP) and hence reduced S/D epi volumes and contact sizes, this is becoming even more stringent. Note that the middle-of-line metal (MOL) plug resistances are not considered in the present analysis. Their importance is also increasing but typically remains a second-order component for ON-current limitation as confirmed in [1].

Due to the limits of existing test-structures (TLM and Kelvin mainly), a new cascaded transistor test-structure (CASC), has been proposed to properly evaluate the R_{access} of real (confined) devices (Fig. 1) and has been utilized since a few years already [6]. By measuring series of adjacent transistors ($\text{NCASC} = 1$ to 4 in the current set-up) and plotting their ON-state resistance (R_{ON}) as a function of the total length ($\text{NCASC} \times \text{CPP}$), it is possible to extract both R_{cont} (offset at $\text{NCASC} \times \text{CPP} = 0$) and $R_{\text{ch}} + R_{\text{epi}} + R_{\text{int}}$ (slope of R vs. $\text{NCASC} \times \text{CPP}$) (Fig. 1(b)), of which R_{ch} is minimized by measuring at large voltage overdrive (V_{OV}).

2. TCAD validation of the access resistance extraction method with cascaded transistor for pFinFET

This extraction methodology is however only valid if the additional channel-to-channel R_{epi} component added when one extra transistor is cascaded ($R_{\text{epi},B}$) is equal to the addition of source-to-channel and channel-to-drain R_{epi} component ($R_{\text{epi},A}$) as illustrated in Fig. 2. To evaluate the CASC extraction method and estimate the potential error margin, we have

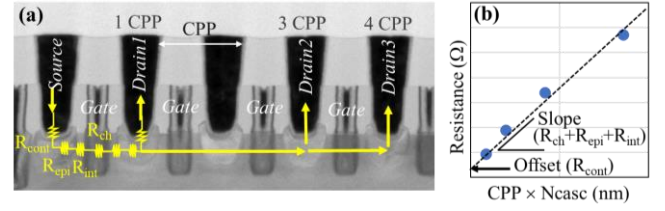


Fig. 1. (a) XTEM view of the CASC test-structure with a schematic representation of the different access resistance components (b) Extraction methodology

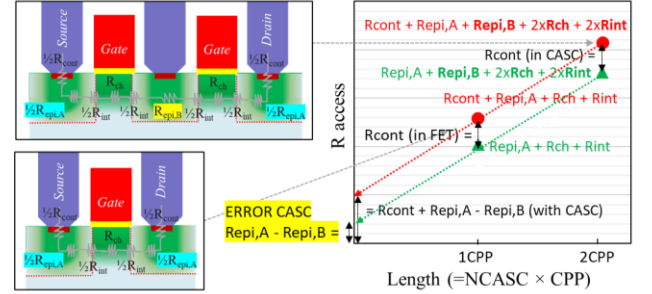


Fig. 2. TCAD verification procedure of the CASC extraction methodology.

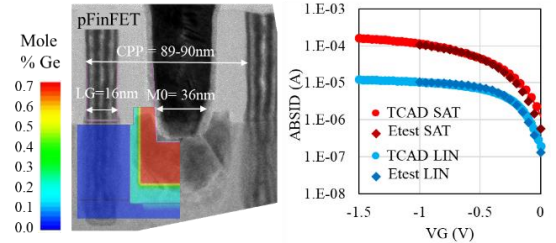


Fig. 3. Calibrated TCAD vs. XTEM and electrical tests (I_D - V_G in linear and saturation regimes respectively) for reference pFinFET

used a calibrated TCAD deck [7] to simulate (i) FET with realistic R_{cont} , (ii) FET with $R_{\text{cont}} = 0$, (iii) CASC (= 2 FETs cascaded) with realistic R_{cont} and (iv) CASC with $R_{\text{cont}} = 0$. This allows to compare R_{cont} extracted on FET and on CASC, and to extract the error margin $R_{\text{epi},A} - R_{\text{epi},B}$ (see Fig. 2).

This methodology was first evaluated on a reference pFinFET device ($\text{CPP} = 90$ nm, $L_G = 16$ nm) with Ge-graded (35% to 65%) SiGe:B S/D epi (Fig. 3). 3D TCAD current density map and normalized R_{ON} at fixed $V_{\text{DD}} = 50$ mV for $V_{\text{OV}} = -1$ V are presented in Fig. 4. In Fig. 5, R_{cont} and $R_{\text{ch}} + R_{\text{epi}} + R_{\text{int}}$ components are shown for 3 different V_{OV} , and the corresponding error margin between reference values extracted on FinFET and with CASC methodology. For $V_{\text{OV}} = -1$ V, this error on R_{cont} extraction with the CASC approach is lower than 4% (Fig. 5(d)).

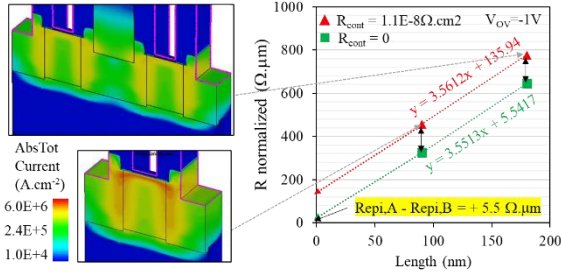


Fig. 4. 3D TCAD current density maps for pFinFET and CASC and verification methodology of the cascaded extraction method.

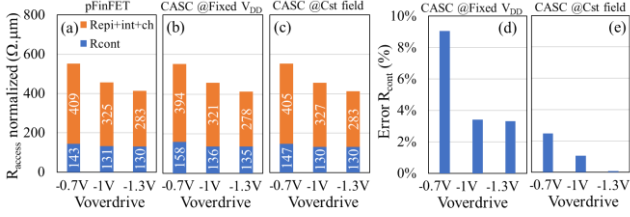


Fig. 5. R_{access} components from TCAD for pFinFET (a) and CASC method (b-c), and error margin varying V_{ov} from -0.7V to -1.3V for fixed V_{DD} (d) and constant field (e).

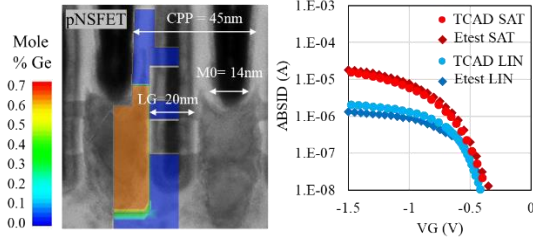


Fig. 6. Calibrated TCAD vs. XTEM and electrical tests ($I_{\text{D}}-V_{\text{G}}$ in linear and saturation regimes respectively) for reference pNSFET

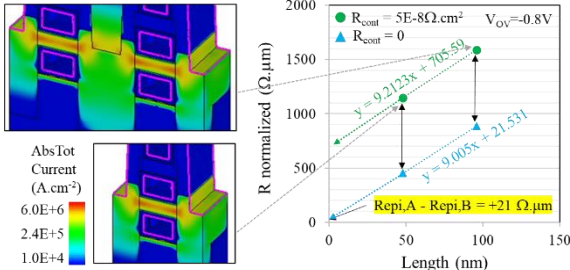


Fig. 7. 3D TCAD current density maps for pNSFET and CASC and verification methodology of the cascaded extraction method.

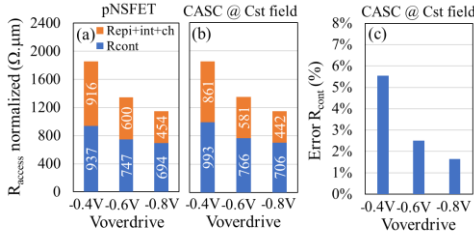


Fig. 8. R_{access} components from TCAD for NSFET (a) and CASC (b) method, and error margin (c) varying V_{ov} from -0.4V to -0.8V

3. Access resistance extraction at constant electrical field

Until now, V_{DD} was kept constant for different NCASC. However, the voltage drop across the different R_{access} components is not the same. This has no impact on purely ohmic components (constant with voltage). Nevertheless, this has an effect on Schottky R_{cont} between metallic local interconnect

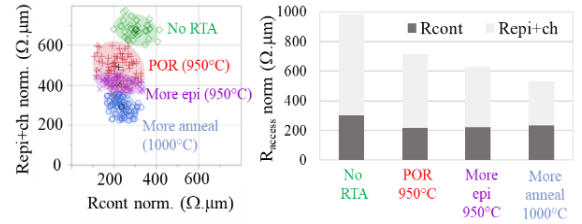


Fig. 9. R_{access} components (clouds and median) extracted with CASC at constant field on nNSFET for different annealing conditions.

and semiconductor epi S/D, and on the heterojunction R_{int} between SiGe S/D epi and Si channel. Hence a refined extraction method is proposed, named constant field method, with V_{DD} modulated as a function of the distance between S and D when NCASC is increased. As illustrated in Fig. 5(e), the error margin is drastically reduced with this approach (already below 1% for $V_{\text{ov}} = -1\text{V}$).

4. TCAD validation for pNSFET

To confirm that our method is also valid for more advanced devices, it was tested on a pNSFET (CPP = 45nm, $L_{\text{G}} = 20\text{nm}$) with $\text{Si}_{0.4}\text{Ge}_{0.6}\text{B}$ epi S/D (Fig. 6). In Figs. 7 and 8, the R_{cont} and $R_{\text{ch}} + R_{\text{epi}} + R_{\text{int}}$ components for different V_{ov} and the corresponding error margin of the CASC extraction method are presented. For $V_{\text{ov}} = -0.8\text{V}$, the error on R_{cont} extraction with CASC approach is reduced to below 2%.

5. Results on nNSFET devices

Finally, we have tested the refined CASC method on nNSFET devices (CPP = 45nm, $L_{\text{G}} = 16\text{nm}$) with Si:P epi S/D, for different post S/D epi growth annealing treatments (no RTA, 950°C and 1000°C for 1.5s). Note that $R_{\text{int}} = 0$ as there is no heterojunction between Si:P S/D epi and Si channel. In Fig. 9 the clouds of R_{cont} and $R_{\text{epi}} + R_{\text{ch}}$ (each point corresponds to a die on the wafer) as well as the median R_{access} after data filtering (details in [6]) are presented. A large positive impact of spike anneal on R_{epi} and smaller on R_{cont} are evidenced resulting from P doping activation and diffusion.

6. Conclusions

The CASC test-structure has been validated and its excellent accuracy to extract different resistance components evidenced with TCAD for both FinFET and NSFET devices. A refined extraction method (at constant field) has been proposed and evaluated with TCAD. First experimental results on nNSFET devices were presented and evidence sensitivity to post S/D epi growth annealing treatments.

Acknowledgements

The imec pilot line, the imec TEM team, and amsimec test labs are acknowledged for their support.

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