SISPAD 2026 Program

Tentative program as of August 28, 2026 (subject to change)

Monday, September 28th, 2026

Opening (Main Hall, 4F)

9:00–9:10 **Opening Remarks**
Hideki Minari (Sony Semiconductor Solutions Corp.)

9:10–9:25 **Welcome Ceremony**

Session PL: Plenary (Main Hall, 4F)

PL-01 (Invited) 9:25–10:10 **Bridging Semiconductor Physics and Device Engineering: From Crystal Anisotropy to Efficient Quantum Transport**
Nobuya Mori[1] (1. The University of Osaka)

PL-02 (Invited) 10:10–10:55 **The EPFL Cryogenic MOSFET Model**
Farzan Jazaeri[1] and Jean-Michel Sallese[1] (1. Ecole Polytechnique Federale de Lausanne (EPFL))

PL-03 (Invited) 10:55–11:40 **From Atom to System: Multi-scale Thermal, Mechanical, and Reliability Modeling of Advanced Packages for AI**
Xi-Wei Lin[1], Ti-Yung Lan[2], Kelly Morgan[1], Xiaopeng Xu[1], Soren Smidstrup[3], Julian Schneider[3] (1. Synopsys Inc.; 2. Synopsys Taiwan; 3. Synopsys Denmark)

Lunch Break (11:40–13:00)

Session 1: Memory Devices (Room A1, 3F)

1-01 (Invited) 13:00–13:30 **From Device Physics to Circuit Co-Design: Multi-Physics Modeling of Monolithic 3D CMOS-NEM Hybrid Circuits**
Woo Young Choi[1] (1. Seoul National University)

1-02 13:30–13:50 **Simulation Study on Scaling Limits of Z-direction Pitch in 3D Flash Memories: Toward the Sub-40 nm Regime**
Tatsuo Ogura[1], Yuma Hizume[1], Yuto Ozeki[1], Takayuki Kakegawa[1], Hiroshi Takeda[1], Takashi Kurusu[1], Tomohiro Oki[1], Katsuyuki Sekine[1] (1. KIOXIA Corp.)

1-03 13:50–14:10 **Vertical Channel-All-Around a-IGZO-FET Towards 2T1D eDRAM Design with Self-Boosted Storage-Node Voltage**
Wenxiang Tang[1,2], Xufan Li[1,2], Yue Zhao[1,2], Xiaoyi Zhang[1,2], Qingxiao Zhu[1,2], Jingrui Guo[3], Lingfei Wang[1,2], Ling Li[1,2] (1. State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences; 2. University of Chinese Academy of Sciences; 3. School of Information Science and Engineering, Shandong University)

1-04 14:10–14:30 **Compact Modeling of the Program Saturation Regime in Charge Trap Flash Memories**
Thomas Hellemans[1,2], Devin Verreck[1,2], Antonio Arreghini[1], Geert Van den Bosch[1], Maarten Rosmeulen[1,2], Michel Houssa[2,1], Jan Van Houdt[1,2] (1. Imec; 2. KU Leuven)

1-05 14:30–14:50 **Enabling 4F² DRAM Junctionless Vertical Channel Transistors with Novel Oxygen Inserted Si Substrates – A TCAD Study**
Albert Lu[1], Madhav Raj[2], Hiu Yung Wong[2], Ilya Rumyantsev[1], Shuyi Li[1], Hideki Takeuchi[1] (1. Atomera Inc.; 2. San Jose State Univ.)

Session 2: Carrier Transport (Room A2, 3F)

2-01 13:10–13:30
Three-Dimensional Quantum Transport in Nanosheet FETs: Effects of Contacts, Geometry, and Multi-Stacks
Seungjin Lee[1], Soyeon Park[1], Seunghyun Song[2], Mincheol Shin[1] (1. Korea Advanced Inst. of Sci. and Tech.; 2. Samsung Electronics)

2-02 13:30–13:50
Alloy-scattering-limited Hole Mobility in SiGe: First-principles-based Multi-scale Approach
Gyeongwon Roh[1], Yeongjun Lim[1], Mincheol Shin[1] (1. Korea Advanced Inst. of Sci. and Tech.)

2-03 13:50–14:10
Framework for Investigating Cryogenic Hole Mobility in Group-IV-Alloy Quantum Wells
Siddhant Sushil Gangwal[1], Shunda Chen[2], Tianshu Li[2], Michael Povolotskyi[3], Dragica Vasileska[1] (1. Arizona State University; 2. George Washington University; 3. Amentum Solutions)

2-04 14:10–14:30
Two-Particle Monte Carlo for TCAD: Fermionic Treatment of Electron–Electron Scattering
Josef Gull[1], Hans Kosina[1] (1. TU Vienna, Inst. for Microelectronics)

2-05 14:30–14:50
Quantum Transport Simulation Considering Self-Energy for Surface Roughness in Nanosheet FETs
Sung-Min Hong[1], Phil-Hun Ahn[2] (1. Gwangju Inst. of Sci. and Tech.; 2. Korea Advanced Inst. of Sci. and Tech.)

Coffee Break (14:50–15:20)

Session 3: Two-Dimensional Materials (Room A1, 3F)

3-01 (Invited) 15:20–15:50
Interface Modeling for TCAD Simulations of 2D Semiconductor Transistors
Akiko Ueda[1] (1. AIST)

3-02 15:50–16:10
Deterministic Full-Band Boltzmann Equation Solver for 2D Materials
Hendrik Christoph Andre Leenders[1], Josephine Faisst[1], Christoph Jungemann[1] (1. RWTH Aachen University)

3-03 16:10–16:30
Engineering of n-type Metal-TMD Contacts via Ferroelectric Polarization: an Ab-initio Transport Study
Alessandro Pilotto[1], Daniel Lizzit[1], Marco Pala[1], David Esseni[1] (1. Univ. of Udine)

3-04 16:30–16:50
Full-Band Semi-Classical Monte Carlo Simulation of Layer Number-Dependent Hole Transport in W- and Mo-Based Transition Metal Dichalcogenides
Donghyeok Lee[1], Sukhyeong Youn[1], Yoonhoo Ha[2], Jiwon Chang[1] (1. Yonsei Univ.; 2. Samsung Adv. Inst. of Tech., Samsung Electronics Co., Ltd.)

3-05 16:50–17:10
Strain-Dependent Electron Transport in Mono-, Bi-, and Trilayer MoS_2 and WS_2 Using Coupled First-Principles and Full-Band Semi-Classical Monte-Carlo Simulation
Seongwoo Kang[1], Yoonhoo Ha[2], Ilgu Yoon[1], Jiwon Chang[1] (1. Yonsei Univ.; 2. Samsung Electronics Cop. Ltd.)

Session 4: Numerical Methods and Algorithms (Room A2, 3F)

4-01 15:30–15:50
Efficient Simulation of Gate Leakage Currents in Ultra-scaled Transistors from First Principles
Mauro Dossena[1], Nicolas Vetsch[1], Alexander Maeder[1], Anders Winka[1], Vincent Maillou[1], Denghui Lu[1], Alexandros Nikolaos Ziogas[1], Jiang Cao[1], Mathieu Luisier[1] (1. Integrated System Laboratory (IIS), ETH Zürich, Switzerland)

4-02 15:50–16:10
Efficient STEM-EBIC Simulation Using an Adjoint Drift-Diffusion Model
Chenyang Yu[1], Sebastian Schneider[2], Bernd Rellinghaus[2], Christoph Jungemann[1] (1. RWTH Aachen Univ.; 2. TUD Dresden Univ. of Tech.)

4-03 16:10–16:30
Harmonic Balance Boltzmann Equation Solver for Gunn Domains
Christoph Jungemann[1] (1. RWTH Aachen University)

4-04 16:30–16:50
Challenges of Drift-Diffusion Simulation for Device Characterization at 4.2 K
Max Renner[1], Yu-Chen Chang[1], Tobias Linn[1], Joachim Knoch[1], Christoph Jungemann[1] (1. RWTH Aachen Univ.)

4-05 16:50–17:10
A TCAD-Friendly Numerical Treatment of Bandtails in Cryogenic and Amorphous Oxide Semiconductors
Mischa Thesberg[1], José María González-Medina[1], Zlatan Stanojević[1], Markus Kampl[1], Franz Schanovsky[1], Oskar Baumgartner[1], Markus Karner[1] (1. Global TCAD Solutions GmbH)

Reception (18:00–20:00, Main Hall Foyer)

Tuesday, September 29th, 2026

Session 5: Atomistic/Ab-initio Modeling (Room A1, 3F)

5-01 (Invited) 9:00–9:30
Atomistic Quantum Transport for the Ångström Era
Philippe Blaise[1] (1. Silvaco Inc.)

5-02 9:30–9:50
SCDMk Wannierization from AO Basis Sets
Fabian Ducry[1], Aryan Afzalian[1] (1. imec be)

5-03 9:50–10:10
Atomistic Insights into NH_3 Plasma-Induced Carbon Depletion and Nitrogen Incorporation in SiCOH Low-K Dielectrics
Sefa Dag[1], El Mehdi Bazizi[1], Subi Kengeri[1], Rohit Gupta[1] (1. Applied Materials, Inc.)

10:10–10:30 **Break**

5-04 10:30–10:50
First-Principles Electrostatic Embedding for Dielectric and Capacitance Analysis in Nonequilibrium 2D Devices
Ryong-Gyu Lee[1], Juho Lee[1], Yong-Hoon Kim[1] (1. Korea Advanced Institute of Science & Technology (KAIST))

5-05 10:50–11:10
Neural-Network-Based Effective-Mass Hamiltonians for Quantum Transport
Geunseok Choi[1], Jooseok Kim[1], Gyeongwon Roh[1], Mincheol Shin[1] (1. KAIST)

5-06 11:10–11:30
Thickness-Dependent Conductivity Scaling of B20-Type Chiral Topological Semimetals for Beyond-Cu Interconnect Applications
Sukhyeong Youn[1], HyeukJin Han[2], Jiwon Chang[1] (1. Yonsei Univ.; 2. Sungshin Womenś Univ.)

5-07 11:30–11:50
DFT-NEGF Modeling of Surface Roughness Scattering in Ultra-Thin-Body Si Nanosheets
Aryan Afzalian[1] (1. imec)

Session 6: Process Simulation (Room A2, 3F)

6-01 9:30–9:50
Unified Lattice Kinetic Monte Carlo Model for Epitaxy, Etch and Reflow Processes for Advanced Semiconductor Device Architectures
Alexander Schmidt[1], Kyungmi Yeom[1], Byounghak Lee[2], Marton Voeroes[2], Hiroyuki Kubotera[2], Woosung Choi[2], Anthony Payet[3], Takeshi Nishimatsu[3], Hiroo Koshimoto[3], Joohyun Jeon[1], Seungmin Lee[1], Jaehoon Jeong[1] (1. Samsung Electronics Co., Ltd; 2. Samsung Semiconductor Inc.; 3. Samsung Device Solutions R&D Japan)

6-02 9:50–10:10
A First-Principles Study of F_2 Selective Etching of Si/SiGe Stacks towards Sub-3 nm Node Transistor Manufacturing
Qikai Zhao[1,2], Junjie Li[1], Hua Shao[1], Rui Chen[1], Lado Filipovic[3] (1. State Key Lab. of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences; 2. School of Integrated Circuits, Univ. of Chinese Academy of Sciences; 3. CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors, Institute for Microelectronics, TU Wien)

10:10–10:30 **Break**

6-03 10:30–10:50
Geometry-Agnostic Feature-Scale PEALD Model
Philipp Haslhofer[1], Tobias Reiter[1], Alexander Toifl[2], Andreas Hóssinger[2], Lado Filipovic[1] (1. Institute for Microelectronics, TU Wien; 2. Silvaco Europe Ltd., Silvaco Inc.)

6-04 10:50–11:10
GPU-Accelerated Feature-Scale Process Simulation of CFET Structures
Tobias Reiter[1], Lado Filipovic[1] (1. Institute for Microelectronics, TU Wien)

6-05 11:10–11:30
Surrogate-Assisted Calibration of a DRIE Process Model
Roman Kostal[1], Manuel Kleinbichler[3], Stefano Di Nicola[4], Lado Filipovic[1,2] (1. Inst. for Microelectronics, Tech. Univ. Vienna; 2. CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors; 3. KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH; 4. Infineon Technologies Austria AG)

Lunch Break (11:30–13:00)

Session 7: Circuit Simulation and Compact Modeling (Room A1, 3F)

7-01 13:00–13:20
Compact Model of Intersubband Coulomb Scattering for FD-SOI Transistors Operating at Cryogenic Temperature
Miltiadis Alepidis[1], Thomas Bédécarrats[1], Aurélie Bajolet[1], Benjamin Dormieu[2], Manohiaina Galal El Dine[2], Patrick Scheer[2], Issa Sidibe[3], Bruna Cardoso Paz[3], Sébastien Martinie[1] (1. Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France; 2. STMicroelectronics, Crolles, France; 3. Quobly, Grenoble, France)

7-02 13:20–13:40
A TCAD-SPICE Simulation Framework for Quantitative Evaluation of MOSFET Properties from SEM Transient Signals
Yuika Kobayashi[1], Yohei Nakamura[1], Shinji Yamaguchi[2] (1. Hitachi, Ltd.; 2. Hitachi High-Tech Corp.)

7-03 13:40–14:00
PrimeSim D2D: A Scalable, Machine Learning-assisted Data-Driven Modeling Framework for Fast DTCO
Chien-Ting Tung Tung[1], Xiaohan Duan[1], Dehuang Wu[1], Joddy Wang[1] (1. Synopsys, Inc.)

Session 8: Quantum Devices (Room A2, 3F)

8-01 13:00–13:20
Device-Consistent Simulation of Spin Exchange Interaction in Quantum Dots Using Green's-Function Method for Inhomogeneous Dielectric Environments
Hidehiro Asai[1], Shota Iizuka[1], Junichi Hattori[1], Tsutomu Ikegami[1], Takashi Nakayama[1], Takahiro Mori[1] (1. National Institute of Advanced Industrial Science and Technology (AIST))

8-02 13:20–13:40
Fast exchange energy simulation in Si spin qubits for point defect variability assessment
Pierre-Louis Julliard[1], Pericles Philippopoulos[2], Tangui Aladjidi[1], Kilian Gruel[1], Etienne Nowak[1], Tristan Meunier[1] (1. Corp. Quobly; 2. Corp. Nanoacademic)

8-03 13:40–14:00
Simulation of Two-qubit Gate Variability and Fidelity of Spin Qubits Built on Nanosheet Technology
Trung Nguyen[1], Sarah Dweik[1], Hiu Yung Wong[1] (1. San Jose State University)

Castle Walking Session (14:15–15:45)

Poster Session (16:00–18:00, Room A3+A4, 3F)

P-01 **Monte Carlo Simulation of the Silicon-Channel Thickness Dependence of Nanosheet Performance**
Fabian Bufler[1], Sylvain Baudot[1], Sheng Yang[1], Philippe Matagne[1], Naoto Horiguchi[1], Geert Hellings[1] (1. IMEC)

P-02 **Multi-subband Monte Carlo Simulation of Scaled Forksheet FETs**
Luca Donetti[1], Cristina Medina-Bailon[1], José Luis Padilla[1], Carlos Sampedro[1], Francisco Gamiz[1] (1. Nanoelectronics Research Group and CITIC, Univ. of Granada, Granada, Spain)

P-03 **Performance Analysis of Silicon GAA-NS-FETs**
Philippe Blaise[1], Daniel Lemus[2], Mark Townsend[1], Eric Guichard[1], Tillmann Kubis[2], Josef Weinbub[1] (1. Silvaco Inc.; 2. Purdue Univ.)

P-04 **Revealing New Leakage Paths in GAAFETs using Predictive First Principle Simulations**
Denis Mamaluy[1] (1. Sandia National Labs)

P-05 **Self-Heating and Radiation Hardness Studies of 3nm GAA-FET-Based SRAM with Different Substrate Isolation Techniques**
Albert Lu[1], Junipero Verbeke[1], Phil Oldiges[2], Reza Arghavani[2], Hiu Yung Wong[1] (1. San Jose State University; 2. Sandia National Laboratories)

P-06 **Circuit-to-Micromagnetics Analysis of Read Disturbance in Two-Terminal SOT-MRAM**
Md Nahid Haque Shazon[1], Cheng-Yu Lin[1], Azad Naeemi[1] (1. Georgia Institute of Technology)

P-08 **TCAD-Based Word Line Driver Optimization for NAND-type 3D Flash Memory Scaling**
Sudarshan Narayanan[1], Qinghua Zhao[1], Satoru Mayuzumi[1], Derek Dou[1], Chao Qin[1], Mohan Dunga[1] (1. Sandisk Technologies Inc.)

P-09 **Avalanche Breakdown in IGBT Corners with VLD Termination: Quantitative 3D TCAD Investigation**
Massimiliano Galvagno[1], Simone Dario Mariani[2], Paola Zuliani[2], Salvatore-Fabio Liotta[3], Silvia Cannizzaro[3], Gerardo Malavena[1], Christian Monzio Compagnoni[1], Alessandro Sottocornola Spinelli[1] (1. Politecnico di Milano; 2. STMicroelectronics; 3. STMicroelectronics)

P-10 **Physics-Informed Compact Modeling of Leakage and Breakdown in GaN-on-Si Devices**
Ilya Rumyantsev[1], Jeff Steinfeldt[2], Nyles Cody[1], Shuyi Li[1], Daniel Connelly[1], Marek Hytha[1], Robert J. Mears[1], Daniel Bailey[3], Jonathan W. Anderson[3], Edwin Piner[3] (1. Atomera Inc.; 2. Sandia National Lab.; 3. Texas State Univ.)

P-11 **SOI PeDMOS R_{ON}-BV-I_{OFF} Tradeoff Optimization through TCAD Simulations**
Joris Lacord[1], Ayoub Boutayeb[2], Dominique Golanski[2], Sylvain Joblot[2], Fabienne Ponthenier[1] (1. CEA-Leti; 2. STMicroelectronics)

P-12 **Double-Gate LDMOS Transistors with Exceptional Figure-of-Merit Exceeding 700 kW/mm²**
Elham Mashhadi[1], William Gerard Vandenberghe[2], Sara Ghazvini[2], Ali Saadat[3], Hal Edwards[4], Sujatha Sampath[4], Daniel Pham[4] (1. The University of Texas at Dallas; 2. The University of Texas at Dallas; 3. Texas Instruments Inc.; 4. Texas Instruments Inc.)

P-13 **Unified TCAD Simulation Framework for InGaAs/InP Single-Photon Avalanche Diodes**
M. Saqlain Khan[1], Andreas Woerl[1], Frank Rutz[1] (1. Fraunhofer-Institute for Applied Solid State Physics IAF)

P-14 **Revisiting Random Dopant Fluctuation at Cryogenic Temperature: the Effect of Incomplete Ionization**
Huawei Tang[1], Yu Wu[1], Junjie Hao[1], Shaofeng Yu[1] (1. Fudan Univ.)

P-15 **Hot Carriers and Self-Heating Effects in FD-SOI Devices at Cryogenic Temperatures**
Bhargav Nallan Chakravartula[1], Ziyi Wang[2], Siddhant Gangwal[1], Katerina Raleva[3], Dragica Vasileska[1], Michael Povolotskyi[4] (1. Arizona State University; 2. onsemi; 3. University Ss Cyril and Methodius; 4. Amentum Solutions)

P-16 **DFT Modeling of O_2-Driven Fragmentation and Islanding from MoS_2 Nanoworms**
Suman Gora[1], Jay Singh[1], Medha Shukla[1], Arnab Datta[1] (1. Indian Institute of Technology (IIT) Roorkee)

P-17 **Modeling and Simulation of Exciton Dynamics in Transition Metal Dichalcogenides Heterostructures**
Rohit Ramesh Nimje[1], Athira S[1], Vignesh S[1], Ashutosh Mahajan[1] (1. Centre for Nanotechnology Research, Vellore Institute of Technology)

P-18 **Analytical SOT MRAM Modeling: From Deterministic to Fokker-Planck based Stochastic Switching**
Trisha Bhowmik[1,2], Maxwel Gama Monteiro[1], Siddharth Rao[1], Yang Xiang[1], Jan Van Houdt[1,2], Kristiaan Temst[1,2], Fernando Garcia Redondo[1], Gouri Sankar Kar[1] (1. Indus.; 2. Univ.)

P-19 **Quasi-Bound State Tunneling in GaN Devices using 2D NEGF with Supercell Mode-Space Method**
Heonseok Oh[1], Phil-Hun Ahn[1], Jooseok Kim[1], Mincheol Shin[1] (1. Korea Advanced Inst. of Sci. and Tech.)

P-20 **Semi-Classical Monte Carlo Simulation of Contact Geometry Effect on Source/Drain Junction Resistance in N-Type Si Fin and Nanosheet FETs**
Uiho Lee[1], Jaeyeon Kim[1], Jiwon Chang[1] (1. Yonsei Univ.)

P-21 **Carrier Density Dependent Transport in Monolayer WS_2**
Nils Vansteenvoort[1,2], Andrés Hidalgo[2], Gautam Gaddemane[2], Bart Sorée[1,2], Maarten L. Van de Put[2] (1. Univ. KU Leuven; 2. Inst. Imec)

P-22 **Lattice-Based Quantum Phonon Transport in FD-SOI Transistors**
David Mai[1], Dirk Schulz[1] (1. TU Dortmund University)

P-23 **FE-NEGF for Cryogenic Thermal Management**
Arnaud Lorin[1], Jing Li[1] (1. Univ. Grenoble Alpes, CEA, Leti)

P-24 **A Fokker-Planck Approach for Modeling Temperature-Dependent Two-Phase Switching Dynamics in Ferroelectrics**
Wei Zhang[1], Leming Jiao[1], Jianze Wang[1], Xiao Gong[1], Xuanyao Fong[1] (1. National Univ. of Singapore)

P-25 **Multi-Stage Etch Recipe Inverse Design: Bridging Expert Behavioral Cloning and Reinforcement Learning**
Jianming Guo[1], Mingqiang Geng[1], Zhengming Liu[2], Dianyu Qi[1], Dong Ni[1], Dawei Gao[1,2] (1. Zhejiang Univ.; 2. Zhejiang ICsprout Semiconductor Co., Ltd.)

P-26 **Layer-by-layer Oxidation of $HfSe_2$ and Formation of Clean van der Waals Interfaces with 2D Semiconductors: A First-Principles Molecular Dynamics Study**
Joonho Park[1], Yong-Hoon Kim[1] (1. Korea Advanced Institute of Sci. and Tech.)

P-27 **Twisting in High Aspect Ratio Etching with Charging Effects as a Stochastic Mechanism**
Taishi Ikeda[1], Hisashi Kotakemori[1], Satoshi Nakamura[1], Kenta Yashima[1], Takumi Ohmura[1], Yasuyuki Kayama[1], YunTae Lee[2], Yukihide Tsuji[2], Shinwook Yi[2], Moon-Hyun Cha[2], Jaehoon Jeong[2] (1. Samsung Japan Corp.; 2. Samsung Electronics Corp.)

P-28 **Impact of Surface Charging on Feature Profile Evolution in 3D NAND Pillar Etching**
Siddharth Mohanty[1], Vatsal Thakor[2], Om Maheshwari[1], Nihar Ranjan Mohapatra[1] (1. Indian Inst. of Tech. Gandhinagar; 2. Nirma Univ.)

P-29 **Pulsed Bias Etching of Silicon Pillar Arrays: Experiment and Surface-Memory Simulation of Loading Control**
Jianming Guo[1], Zhengming Liu[2], Mingqiang Geng[1], Kunrun Song[2], Huiyun Jiang[1,2], Dong Ni[1], Dawei Gao[1,2] (1. Zhejiang Univ.; 2. Zhejiang ICsprout Semiconductor Co., Ltd.)

P-30 **Experiment-Based Modeling of Wafer-to-Wafer Bonding for 3D Integration**
Hyuga Ishii[1], Takashi Shimura[2], Ryota Ogata[1], Hayato Kitagawa[1], Taisuke Yamamoto[1], Fumihiro Inoue[1] (1. Yokohama National University; 2. ESTECH Corp.)

P-31 **OPC+: GPU-Accelerated Lithography Simulation with Contour-Based Calibration and Unified Inverse Mask Optimization**
Po-Hsun Fang[1], Pokai Chang[1], Kuan-Hsun Wang[1], Zhi-Sheng Wang[1], Han-Xuan Huang[1], Shie-Yuan Wang[1], Peichen Yu[1] (1. National Yang Ming Chiao Tung Univ.)

P-32 **Multi-Phase-Field Modeling of Thin-Film Silicidation**
Christophe Pixius[1], Ferdinand Schulz[1], Sanjukta Chowdhury[1], Eberhard Baer[1], Christopher Straub[1], Andreas Rosskopf[1] (1. Fraunhofer IISB)

P-33 **SEMulator3D® Linking Deposition Process to Electrical Metrics-Accelerated WAT Learning**
Xing Qin[1], Tristan Yang[1], Deyong Kong[1], Xiaoqiang Wan[1] (1. Lam Research Corp.)

P-34 **SPER-Driven Dislocation Nucleation and Uphill Diffusion Modeling for Advanced Semiconductor Processing**
Chihak Ahn[1], Alexander Schmidt[2], Joohyun Jeon[2], Seungmin Lee[2], Woosung Choi[1], Jaehoon Jeong[2] (1. Samsung Semiconductor Inc.; 2. Samsung Electronics)

P-35 **Feature Charging During Cryogenic Plasma Etching**
Yeon Geun Yook[1], Chenyao Huang[1], Yifan Gui[1], Mark J. Kushner[1] (1. Univ. of Michigan)

P-36 **A Covariance Matrix Adaptation Evolutionary Strategy Parameter Extractor for BSIM-CMG**
Jen-Hao Chen[1], Ahtisham Pampori[1], Chenming Hu[1], Sayeef Salahuddin[1] (1. Univ. of California, Berkeley)

P-37 **An Accurate Temperature-Dependent Compact Model for Ferroelectric Capacitors**
Nandakishor Yadav[1], Phuoc Khang Nguyen[1], Maximilian Lederer[1], Jacob Syndikus[1], Tianren Zhang[1], David Lehninger[1], Konrad Seidel[1], Thomas Kaempfe[1] (1. Fraunhofer Institute for Photonic Microsystems IPMS Dresden)

P-38 **Comprehensive SPICE Compact Modeling of Split-Gate Embedded Flash Memory for Transient and Worst-Case Operation Failure Simulation**
Dongwoo Lim[1,2], Kiyoung Kim[2], Hyungcheol Shin[1] (1. Seoul National Univ.; 2. Samsung Electronics Co., Ltd.)

P-39 **SPICE Modeling Method of Reverse Recovery Based on TCAD Analysis**
Emiru Baba[1], Shigeru Nakajima[1], Tsuyoshi Kachi[1], Takuma Hara[1], Kozo Kinoshita[1] (1. Toshiba Electronic Devices & Storage Corporation)

P-40 **First-principles Calculation of Free Carrier Absorption in 4H-SiC**
Masahiko Matsubara[1], Enrico Bellotti[1] (1. Boston University)

P-41 **Low-temperature Enhancement of Quantum Hybridization-Induced Negative Differential Resistance in a Pb-free 1D Halide Perovskite**
Jeongwon Lee[1], Tae Hyung Kim[1], Juho Lee[1], Yong-Hoon Kim[1] (1. Korea Advanced Inst. of Sci. and Tech.)

P-42 **Multi-space Density Functional Simulations of WSe_2 p-n Junctions**
Hyeonjun Kang[1], Taehyung Kim[1], Juho Lee[1], Ryonggyu Lee[1], Yonghoon Kim[1] (1. Korea Advanced Institute of Sci. and Tech. (KAIST))

P-43 **Machine Learning Framework for the Inverse Design of Tight-Binding Parameters in Compound Semiconductors**
Kaito Seike[1], Shingo Sato[1] (1. Kansai University)

P-44 **A Machine-Learning Accelerated Atom-to-Transistor Simulation Framework**
Pratik Brahma[1], Krishna Bhattaram[1], Sayeef Salahuddin[1] (1. University of California, Berkeley)

P-45 **Physics-Enhanced LSTM Modeling of Electric Double-Layer Transistors**
Haoran Yang[1,2], Shuaidi Zhang[1,2], Yue Zhao[1,2], Ling Li[1,2] (1. Inst. of Microelectronics, CAS; 2. Univ. of CAS)

P-46 **Power–Performance Assessment of 48 nm Gate-Pitch CFETs Using Experimentally Calibrated Physics-Informed ANN Models**
Yu-Wen Xu[1], Yiming Li[1], Min-Hui Chuang[1], Yun Tai[1] (1. National Yang Ming Chiao Tung Univ.)

P-47 **AI-driven TCAD Surrogate Modeling and Multi-Objective Optimization for Accelerated Technology Development**
Derek Dou[1], Sudarshan Narayanan[1], Qinghua Zhao[1], Chao Qin[1], Mohan Dunga[1] (1. Sandisk Tech., Inc.)

P-48 **Accelerating Simulation of General Gate-All-Around Transistors via a Quasi-1D Model**
Gyubeen Kim[1], Kwang-Woon Lee[2], Sung-Min Hong[2] (1. Department of Semiconductor Eng., Gwangju Inst. of Sci. and Tech.; 2. Department of Electrical Eng. and Computer Sci., Gwangju Inst. of Sci. and Tech.)

P-49 **Machine Learning Accelerated Geometry Optimization under External Electric Fields**
Yuanchen Chu[1], Guido Gandus[1], Kantawong Vuttivorakulchai[2], Marton Voeroes[1], Hong-Hyun Park[1], MinYong Jeong[2], Mohammad Ali Pourghaderi[2], Uihui Kwon[2], Yoon-Suk Kim[2], Seungmin Lee[2], Woosung Choi[1], Jaehoon Jeong[2] (1. TCAD lab, Samsung Semiconductor Inc.; 2. Computational Sci. and Engineering Team, Samsung Electronics)

Wednesday, September 30th, 2026

Session 9: Advanced CMOS Devices (Room A1, 3F)

9-01 (Invited) 9:00–9:30 **Efficient DC Simulation of Monolithic CFETs Using a Quasi-1D Approach**
Sung-Min Hong[1] (1. Gwangju Institute of Science and Technology)

9-02 9:30–9:50 **Impact of 4F2 DRAM Access Transistor Design on Floating Body Effect and Retention**
Ashish Pal[1], Lars P. Tatum[1], Rohit Gupta[1], El Mehdi Bazizi[1], Subi Kengeri[1] (1. Applied Materials)

9-03 9:50–10:10 **Multiscale Modeling of Channel Surface Roughness: Impact on Front-End-of-Line And Circuit Performance for Advanced Logic Technology**
Ning Yang[1], Pratik B. Vyas[1], Rohit Gupta[1], Ashish Pal[1], El Mehdi Bazizi[1], Subi Kengeri[1] (1. Applied Materials Inc.)

10:10–10:30 **Break**

9-04 10:30–10:50 **Impact of Thermal Expansion Mismatch-Induced NMOS Metal Gate Stress on MBCFET Performance**
Sung-Ho Kim[1], Sooyoung Park[1], Chang Ju Moon[1], Jong Su Kim[1], Jaehong Lee[1], Yoon-Suk Kim[1], Seung Hyun Song[1], Yonghee Park[1], Jaehoon Jeong[1] (1. Samsung Electronics Corp., Ltd.)

9-05 10:50–11:10 **Modeling of Soft Errors in CFET SRAM Using Machine Learning-Assisted Circuit Simulation**
Vanness Filbert Cierra[1], Yoshinari Kamakura[1] (1. Osaka Inst. Tech.)

9-06 11:10–11:30 **Low-Temperature Behavior in Silicon Nanowire n-FETs Studied by Atomistic NEGF**
Sanam Moslemi-Tabrizi[2], Peter Schvan[2], Philippe Blaise[1], Udita Kapoor[1], Daniel Lemus[3], Tillmann Kubis[3] (1. Silvaco Inc.; 2. Ciena Inc.; 3. Purdue Univ.)

Session 10: Defects, Reliability and Variability (Room A2, 3F)

10-01 9:10–9:30 **Multi-Scale Statistical Modeling of Random Telegraph Noise in Sub-Micrometer CIS**
Jae Ho Kim[1], Sungchul Kim[1], Yonghee Park[1], Jonhyun Go[1], Jae Hoon Jung[1] (1. Samsung Electronics)

10-02 9:30–9:50 **Antisite Disorder in the Native Oxide Insulator β-Bi_2SeO_5: A First-Principles Study**
Mina Bahrami Bahrami[1], Mohammad Rasool Davoudi[1], Dominic Waldhoer[1], Christoph Wilhelmer[1], Pedram Khakbaz[1], Theresia Knobloch[1], Michael Waltl[1], Tibor Grasser[1] (1. Institute for Microelectronics)

10-03 9:50–10:10
A Unified Physical Model for Bias Temperature Instability in OSFETs
Yongjia Wang[1], Haotong Zhu[1], Jinghan Xu[1], Ligong Zhang[1], Jinfeng Kang[1], Xiaoyan Liu[1] (1. Peking Univ.)

10:10–10:30 **Break**

10-04 10:30–10:50
Modeling the Memory Window Distribution in FeFETs Considering Grain Variability
Kenichiro Sonoda[1], Shibun Tsuda[1], Tadashi Yamaguchi[1], Atsushi Amo[1], Eiji Tsukuda[1] (1. Renesas Electronics Corp.)

10-05 10:50–11:10
Modeling Counterclockwise Current Hysteresis in Oxide Thin-Film Transistors
Pranay Baikadi[1], Benius Dunn[1], Sara Ghazvini[1], Julia W. P. Hsu[1], William G. H. Vandenberghe[1] (1. University of Texas at Dallas)

10-06 11:10–11:30
Disentangling Hysteresis in Emerging Transistors: Beyond Threshold Shifts to Area-Based Decomposition
Mohammad Rasool Davoudi[1], Dominic Waldhoer[1], Mina Bahrami[1], Alexander Karl[1], Pedram Khakbaz[1], Axel Verdianu[1], Michael Waltl[1], Theresia Knobloch[1], Tibor Grasser[1] (1. TU Wien (Technische Universität Wien))

10-07 11:30–11:50
First-Principles Evaluation of *p*-type Conductivity in Zn-Doped Bismuth Oxyselenide (Bi_2O_2Se)
Christoph Wilhelmer[1], Tibor Grasser[1] (1. TU Wien)

Lunch Break (11:30–13:00)

Session 11: Artificial Intelligence and Machine Learning (Room A1, 3F)

11-01 13:00–13:20
Atomistic Modeling of Mg-Ion Implantation into GaN using an Efficient Machine-Learned Interatomic Potential
Yuki Ohuchi[1,3], Robert Stella[2,3], Sabine Leroch[2,3], Lado Filipovic[2,3] (1. Advanced Technology Laboratory, Fuji Electric Corp. Ltd.; 2. CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors; 3. Inst. for Microelectronics, TU Wien)

11-02 13:20–13:40
***k-space* resolved surrogate models for efficient inverse design of optical metasurfaces**
Damien Maitre[1,2], Francesco Guadagnuolo[1], Jean-Philippe Banon[2], Maxime Darnon[2], Raphaël Clerc[2], Loumi Tremas[1], Mathys Le Grand[1], Adam Fuchs[1], Pascal Urard[1], Coumba Gaye[1], Olivier Jeannin[1], James Downing[1], Denis Rideau[1] (1. STMicroelectronics; 2. Univ. Jean Monnet, CNRS, Institut d Optique Graduate School)

11-03 13:40–14:00
Physics-Informed Neural Networks for Stable Drift-Diffusion Simulation and Inverse Parameter Extraction in 2D Semiconductors Devices
Satofumi Souma[1], Akiko Ueda[2] (1. Kobe Univ.; 2. AIST)

11-04 14:00–14:20
A Deep Learning Framework for Fast, Unified Process and Device TCAD Simulation
Konstantina Kovani[1], Greta Chiaravalli[1], Francesco Di Stefano[1], Michal Dyrek[1], Semin Kwak[1], Vamsi Spandan Arza[1], Ryota Hachiya[2], Yonggwi Cho[2], Hideki Minari[2], Jun Komachi[2], Shinya Yamakawa[2], Lorenzo Servadei[1] (1. AI for Chip Design Team, Sony AI, Zurich; 2. Sony Semiconductor Solutions Corp., Tokyo, Japan)

Session 12: Thermal Transport and Electro-Thermal Modeling (Room A2, 3F)

12-01 13:00–13:20
A Novel 2.5D Thermal Coupling Model for Device/Metal Reliability Applications
Jyun-Yan Kuo[1], Gary Lee[1], Kasa Huang[1], Jeffrey Tzeng[1], Y.S. Lin[1], S.H. Li[1], Y.L. Chang[1], H.P. Chien[1], P.C. Hsu[1], G.T. Lin[1], W.C. Chang[1], Eugene Chen[1], C. C. Lai[1], Tony Yu[1], M.H. Hsieh[1], Clement Huang[1], K.Y. Su[1], Jim Liang[1], K.W. Su[1], C.K. Lin[1] (1. Taiwan Semiconductor Manufac. Company)

12-02 13:20–13:40
Joule heating and thermal transport in 2D materials for device applications
Zlatan Aksamija[1], Sylvester Makumi[1], Aidan Belanger[1] (1. Univ. of Utah)

12-03 13:40–14:00
Monte Carlo Modeling of Phonon Drag Effects on Thermoelectric Transport in Silicon Nanostructures with doping modulation
Jerome Saint-Martin[1,2], Mohammad Ghanem[1], Raja Sen[3], Jelena Sjakste[3], Philippe Dollfus[1] (1. Université Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies; 2. Université Paris-Saclay, ENS Paris-Saclay, CNRS, SATIE; 3. Laboratoire des Solides Irradiés, CEA-DRF-IRAMIS, École Polytechnique)

12-04 14:00–14:20
Three-Dimensional Monte Carlo Simulation of Phonon Transport in Amorphous IGZO Thin-Film Transistors
Chenglin Ye[1], Zhaoxing Yan[1], Haotong Zhu[1], Ligong Zhang[1], Yuanzhao Hu[1], Xiaoyan Liu[1] (1. Peking Univ.)

Closing (14:30–14:45, Room A1, 3F)