

SISPAD 2026 Program

Monday, September 28, 2026 (Kumamoto-Jo Hall)

Opening (Main Hall, 4F)

9:00 - 9:25 **Opening Remarks**
Hideki Minari (Sony Semiconductor Solutions Corp.)

Session PL: Plenary (Main Hall, 4F)

Chairpersons: Kai Tak Lam (TSMC)
Hajime Tanaka (Kwansei Gakuin Univ.)

PL-01 9:25 - 10:10 **[invited talk]**

Bridging Semiconductor Physics and Device Engineering: From Crystal Anisotropy to Efficient Quantum Transport
Nobuya Mori¹ (¹The University of Osaka)

PL-02 10:10 - 10:55 **[invited talk]**

The EPFL Cryogenic MOSFET Model
Farzan Jazaeri¹, Jean-Michel Sallese¹ (¹Swiss Federal Institute of Technology in Lausanne)

PL-03 10:55 - 11:40 **[invited talk]**

From Atom to System: Multi-scale Thermal, Mechanical, and Reliability Modeling of Advanced Packages for AI

Xi-Wei Lin¹, Ti-Yung Lan², Kelly Morgan¹, Xiaopeng Xu¹, Soren Smidstrup³, Julian Schneider³
(¹Synopsys Inc., ²Synopsys Taiwan, ³Synopsys Denmark)

11:40 - 13:00 Lunch Break (Room A3+A4, 3F)

Session 1: Memory Devices (Room A1, 3F)

Chairpersons: Kenichiro Sonoda (Renesas)
Hiroshi Takeda (Kioxia)

1-01 13:00 - 13:30 **[invited talk]**

From Device Physics to Circuit Co-Design: Multi-Physics Modeling of Monolithic 3D CMOS-NEM Hybrid Circuits
Woo Young Choi¹ (¹Seoul National University)

1-02 13:30 - 13:50

Simulation Study on Scaling Limits of Z-direction Pitch in 3D Flash Memories: Toward the Sub-40 nm Regime

Tatsuo Ogura¹, Yuma Hizume¹, Yuto Ozeki¹, Takayuki Kakegawa¹, Hiroshi Takeda¹, Takashi Kurusu¹, Tomohiro Oki¹, Katsuyuki Sekine¹ (¹KIOXIA Corp.)

1-03 13:50 - 14:10

Vertical Channel-All-Around a-IGZO-FET Towards 2T1D eDRAM Design with Self-Boosted Storage-Node Voltage

Wenxiang Tang^{1,2}, Xufan Li^{1,2}, Yue Zhao^{1,2}, Xiaoyi Zhang^{1,2}, Qingxiao Zhu^{1,2}, Jingrui Guo³, Lingfei Wang^{1,2}, Ling Li^{1,2} (¹State Key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, ²University of Chinese Academy of Sciences, ³School of Information Science and Engineering, Shandong University)

1-04 14:10 - 14:30

Compact Modeling of the Program Saturation Regime in Charge Trap Flash Memories

Thomas Hellemans^{1,2}, Devin Verreck^{1,2}, Antonio Arreghini¹, Geert Van den bosch¹, Maarten Rosmeulen^{1,2}, Michel Houssa^{2,1}, Jan Van Houdt^{1,2} (¹Imec, ²KU Leuven)

- 1-05** 14:30 - 14:50
 Enabling 4F² DRAM Junctionless Vertical Channel Transistors with Novel Oxygen Inserted Si Substrates – A TCAD Study
Albert Lu¹, Madhav Raj², Hui Yung Wong², Ilya Rumyantsev¹, Shuyi Li¹, Hideki Takeuchi¹ (¹Atomera Inc., ²San Jose State Univ.)

Session 2: Carrier Transport (Room A2, 3F)

- Chairpersons: François Triozon (CEA-Leti)
Shingo Sato (Kansai Univ.)
- 2-01** 13:10 - 13:30
 Three-Dimensional Quantum Transport in Nanosheet FETs: Effects of Contacts, Geometry, and Multi-Stacks
Seungjin Lee¹, Soyeon Park¹, Seunghyun Song², Mincheol Shin¹ (¹Korea Advanced Inst. of Sci. and Tech., ²Samsung Electronics)
- 2-02** 13:30 - 13:50
 Alloy-scattering-limited Hole Mobility in SiGe: First-principles-based Multi-scale Approach
Gyeongwon Roh¹, Yeongjun Lim¹, Mincheol Shin¹ (¹Korea Advanced Inst. of Sci. and Tech.)
- 2-03** 13:50 - 14:10
 Framework for Investigating Cryogenic Hole Mobility in Group-IV-Alloy Quantum Wells
Siddhant Sushil Gangwal¹, Shunda Chen², Tianshu Li², Michael Povolotskyi³, Dragica Vasileska¹
 (¹Arizona State University, ²George Washington University, ³Amentum Solutions)
- 2-04** 14:10 - 14:30
 Two-Particle Monte Carlo for TCAD: Fermionic Treatment of Electron–Electron Scattering
Josef Gull¹, Hans Kosina¹ (¹TU Vienna, Inst. for Microelectronics)
- 2-05** 14:30 - 14:50
 Quantum Transport Simulation Considering Self-Energy for Surface Roughness in Nanosheet FETs
Sung-Min Hong¹, Phil-Hun Ahn² (¹Gwangju Inst. of Sci. and Tech., ²Korea Advanced Inst. of Sci. and Tech.)
- 14:50 - 15:20 Coffee Break (Exhibition Area, Foyer, 3F)

Session 3: Two-Dimensional Materials (Room A1, 3F)

- Chairpersons: William Vandenberghe (UT Dallas)
Satofumi Souma (Kobe Univ.)
- 3-01** 15:20 - 15:50 **[invited talk]**
 Interface Modeling for TCAD Simulations of 2D Semiconductor Transistors
Akiko Ueda¹ (¹AIST)
- 3-02** 15:50 - 16:10
 Deterministic Full-Band Boltzmann Equation Solver for 2D Materials
Hendrik Christoph Andre Leenders¹, Josephine Faisst¹, Christoph Jungemann¹ (¹RWTH Aachen University)
- 3-03** 16:10 - 16:30
 Engineering of n-type Metal-TMD Contacts via Ferroelectric Polarization: an Ab-initio Transport Study
Alessandro Pilotto¹, Daniel Lizzit¹, Marco Pala¹, David Esseni¹ (¹Univ. of Udine)
- 3-04** 16:30 - 16:50
 Full-Band Semi-Classical Monte Carlo Simulation of Layer Number-Dependent Hole Transport in W- and Mo-Based Transition Metal Dichalcogenides
Donghyeok Lee¹, Sukhyeong Youn¹, Yoonhoo Ha², Jiwon Chang¹ (¹Yonsei Univ., ²Samsung Adv. Inst. of Tech., Samsung Electronics Co., Ltd.)

3-05 16:50 - 17:10

Strain-Dependent Electron Transport in Mono-, Bi-, and Trilayer MoS₂ and WS₂ Using Coupled First-Principles and Full-Band Semi-Classical Monte-Carlo Simulation
Seongwoo Kang¹, Yoonhoo Ha², Ilgu Yoon¹, Jiwon Chang¹ (¹Yonsei Univ., ²Samsung Electronics Cop. Ltd.)

Session 4: Numerical Methods and Algorithms (Room A2, 3F)

Chairpersons: Sung-Min Hong (GIST)
Shunsuke Koba (Kobe City Col. Tech.)

4-01 15:30 - 15:50

Efficient Simulation of Gate Leakage Currents in Ultra-scaled Transistors from First Principles
Mauro Dossena¹, Nicolas Vetsch¹, Alexander Maeder¹, Anders Winka¹, Vincent Maillou¹, Denghui Lu¹, Alexandros Nikolaos Ziogas¹, Jiang Cao¹, Mathieu Luisier¹ (¹Integrated System Laboratory (IIS), ETH Zürich, Switzerland)

4-02 15:50 - 16:10

Efficient STEM-EBIC Simulation Using an Adjoint Drift-Diffusion Model
Chenyang Yu¹, Sebastian Schneider², Bernd Rellinghaus², Christoph Jungemann¹ (¹RWTH Aachen Univ., ²TUD Dresden Univ. of Tech.)

4-03 16:10 - 16:30

Harmonic Balance Boltzmann Equation Solver for Gunn Domains
Christoph Jungemann¹ (¹RWTH Aachen University)

4-04 16:30 - 16:50

Challenges of Drift-Diffusion Simulation for Device Characterization at 4.2 K
Max Renner¹, Yu-Chen Chang¹, Tobias Linn¹, Joachim Knoch¹, Christoph Jungemann¹ (¹RWTH Aachen Univ.)

4-05 16:50 - 17:10

A TCAD-Friendly Numerical Treatment of Bandtails in Cryogenic and Amorphous Oxide Semiconductors
Mischa Thesberg¹, José María González-Medina¹, Zlatan Stanojević¹, Markus Kampl¹, Franz Schanovsky¹, Oskar Baumgartner¹, Markus Karner¹ (¹Global TCAD Solutions GmbH)

18:00 - 20:00 Reception (Main Hall Foyer, 4F)

Tuesday, September 29, 2026 (Kumamoto-Jo Hall)

Session 5: Atomistic/Ab-initio Modeling (Room A1, 3F)

Chairpersons: Zlatan Aksamija (Univ. of Utah)
Yuki Ohuchi (Fuji Electric)

5-01 9:00 - 9:30 [invited talk]

Atomistic Quantum Transport for the Ångström Era
Philippe Blaise¹ (¹Silvaco Inc.)

5-02 9:30 - 9:50

SCDMk Wannierization from AO Basis Sets
Fabian Ducry¹, Aryan Afzalian¹ (¹imec be)

5-03 9:50 - 10:10

Atomistic Insights into NH₃ Plasma-Induced Carbon Depletion and Nitrogen Incorporation in SiCOH Low-K Dielectrics
Sefa Dag¹, El Mehdi Bazizi¹, Subi Kengeri¹, Rohit Gupta¹ (¹Applied Materials, Inc.)

10:10 - 10:30 Coffee Break (Exhibition Area, Foyer, 3F)

- 5-04** 10:30 - 10:50
First-Principles Electrostatic Embedding for Dielectric and Capacitance Analysis in Nonequilibrium 2D Devices
Ryong-Gyu Lee¹, Juho Lee¹, Yong-Hoon Kim¹ (¹Korea Advanced Institute of Science & Technology (KAIST))
- 5-05** 10:50 - 11:10
Neural-Network-Based Effective-Mass Hamiltonians for Quantum Transport
Geunseok Choi¹, Jooseok Kim¹, Gyeongwon Roh¹, Mincheol Shin¹ (¹KAIST)
- 5-06** 11:10 - 11:30
Thickness-Dependent Conductivity Scaling of B20-Type Chiral Topological Semimetals for Beyond-Cu Interconnect Applications
Sukhyeong Youn¹, HyeukJin Han², Jiwon Chang¹ (¹Yonsei Univ., ²Sungshin Women's Univ.)
- 5-07** 11:30 - 11:50
DFT-NEGF Modeling of Surface Roughness Scattering in Ultra-Thin-Body Si Nanosheets
Aryan Afzalian¹ (¹imec)

Session 6: Process Simulation (Room A2, 3F)

Chairpersons: Sung-Min Hong (GIST)
Hiroki Tokuhira (Kioxia)

- 6-01** 9:30 - 9:50
Unified Lattice Kinetic Monte Carlo Model for Epitaxy, Etch and Reflow Processes for Advanced Semiconductor Device Architectures
Alexander Schmidt¹, Kyungmi Yeom¹, Byounghak Lee², Marton Voeroes², Hiroyuki Kubotera², Woosung Choi², Anthony Payet³, Takeshi Nishimatsu³, Hiroo Koshimoto³, Joohyun Jeon¹, Seungmin Lee¹, Jaehoon Jeong¹ (¹Samsung Electronics Co., Ltd, ²Samsung Semiconductor Inc., ³Samsung Device Solutions R&D Japan)
- 6-02** 9:50 - 10:10
A First-Principles Study of F₂ Selective Etching of Si/SiGe Stacks towards Sub-3 nm Node Transistor Manufacturing
Qikai Zhao^{1,2}, Junjie Li¹, Hua Shao¹, Rui Chen¹, Lado Filipovic³ (¹State Key Lab. of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, ²School of Integrated Circuits, Univ. of Chinese Academy of Sciences, ³CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors, Institute for Microelectronics, TU Vienna)
10:10 - 10:30 Coffee Break (Exhibition Area, Foyer, 3F)
- 6-03** 10:30 - 10:50
Geometry-Agnostic Feature-Scale PEALD Model
Philipp Haslhofer¹, Tobias Reiter¹, Alexander Toifl², Andreas Hössinger², Lado Filipovic¹ (¹Institute for Microelectronics, TU Wien, ²Silvaco Europe Ltd., Silvaco Inc.)
- 6-04** 10:50 - 11:10
GPU-Accelerated Feature-Scale Process Simulation of CFET Structures
Tobias Reiter¹, Lado Filipovic¹ (¹Institute for Microelectronics, TU Wien)
- 6-05** 11:10 - 11:30
Surrogate-Assisted Calibration of a DRIE Process Model
Roman Kostal¹, Manuel Kleinbichler³, Stefano Di Nicola⁴, Lado Filipovic^{1,2} (¹Inst. for Microelectronics, Tech. Univ. Vienna, ²CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors, ³KAI Kompetenzzentrum Automobil- und Industrielektronik GmbH, ⁴Infineon Technologies Austria AG)
11:30 - 13:00 Lunch Break (Room A3+A4, 3F)

Session 7: Circuit Simulation and Compact Modeling (Room A1, 3F)

Chairpersons: Nobuhiko Nakano (Keio Univ.)
Kenichiro Sonoda (Renesas)

- 7-01** 13:00 - 13:20
Compact Model of Intersubband Coulomb Scattering for FD-SOI Transistors Operating at Cryogenic Temperature
Miltiadis Alepidis¹, Thomas Bédécarrats¹, Aurélie Bajolet¹, Benjamin Dormieu², Manohiaina Galal El Dine², Patrick Scheer², Issa Sidibe³, Bruna Cardoso Paz³, Sébastien Martinie¹ (¹Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France, ²STMicroelectronics, Crolles, France, ³Quobly, Grenoble, France)
- 7-02** 13:20 - 13:40
A TCAD-SPICE Simulation Framework for Quantitative Evaluation of MOSFET Properties from SEM Transient Signals
Yuika Kobayashi¹, Yohei Nakamura¹, Shinji Yamaguchi² (¹Hitachi, Ltd., ²Hitachi High-Tech Corp.)
- 7-03** 13:40 - 14:00
PrimeSim D2D: A Scalable, Machine Learning-assisted Data-Driven Modeling Framework for Fast DTCO
Chien-Ting Tung¹, Xiaohan Duan¹, Dehuang Wu¹, Joddy Wang¹ (¹Synopsys, Inc.)

Session 8: Quantum Devices (Room A2, 3F)

- Chairpersons: Jaehyun Lee (Pusan National Univ.)
Satofumi Souma (Kobe Univ.)
- 8-01** 13:00 - 13:20
Device-Consistent Simulation of Spin Exchange Interaction in Quantum Dots Using Green's-Function Method for Inhomogeneous Dielectric Environments
Hidehiro Asai¹, Shota Iizuka¹, Junichi Hattori¹, Tsutomu Ikegami¹, Takashi Nakayama¹, Takahiro Mori¹ (¹National Institute of Advanced Industrial Science and Technology (AIST))
- 8-02** 13:20 - 13:40
Fast exchange energy simulation in Si spin qubits for point defect variability assessment
Pierre-Louis Julliard¹, Pericles Philippopoulos², Tangui Aladjidi¹, Kilian Gruel¹, Etienne Nowak¹, Tristan Meunier¹ (¹Corp. Quobly, ²Corp. Nanoacademic)
- 8-03** 13:40 - 14:00
Simulation of Two-qubit Gate Variability and Fidelity of Spin Qubits Built on Nanosheet Technology
Trung Nguyen¹, Sarah Dweik¹, Hiu Yung Wong¹ (¹San Jose State University)
- 14:15 - 15:45 Castle Walking Session (Kumamoto Castle)

Poster Session (Room A3+A4, 3F)

- Chairpersons: Shingo Sato (Kansai Univ.)
Shotaro Nishiura (Sony)
- 16:00 - 17:00 Presentation time for the odd-numbered poster
17:00 - 18:00 Presentation time for the even-numbered poster
- P-01** Monte Carlo Simulation of the Silicon-Channel Thickness Dependence of Nanosheet Performance
Fabian Bufler¹, Sylvain Baudot¹, Sheng Yang¹, Philippe Matagne¹, Naoto Horiguchi¹, Geert Hellings¹ (¹IMEC)
- P-02** Multi-subband Monte Carlo Simulation of Scaled Forksheet FETs
Luca Donetti¹, Cristina Medina-Bailon¹, José Luis Padilla¹, Carlos Sampedro¹, Francisco Gamiz¹ (¹Nanoelectronics Research Group and CITIC, Univ. of Granada, Granada, Spain)
- P-03** Performance Analysis of Silicon GAA-NS-FETs
Philippe Blaise¹, Daniel Lemus², Mark Townsend¹, Eric Guichard¹, Tillmann Kubis², Josef Weinbub¹ (¹Silvaco Inc., ²Purdue Univ.)
- P-04** Revealing New Leakage Paths in GAAFETs using Predictive First Principle Simulations
Denis Mamaluy¹ (¹Sandia National Labs)

- P-05** Self-Heating and Radiation Hardness Studies of 3nm GAA-FET-Based SRAM with Different Substrate Isolation Techniques
Albert Lu¹, Junipero Verbeke¹, Phil Oldiges², Reza Arghavani², Hiu Yung Wong¹ (¹San Jose State University, ²Sandia National Laboratories)
- P-06** Circuit-to-Micromagnetics Analysis of Read Disturbance in Two-Terminal SOT-MRAM
MD NAHID HAQUE SHAZON¹, Cheng-Yu Lin¹, Azad Naeemi¹ (¹Georgia Institute of Technology)
- P-08** TCAD-Based Word Line Driver Optimization for NAND-type 3D Flash Memory Scaling
Sudarshan Narayanan¹, Qinghua Zhao¹, Satoru Mayuzumi¹, Derek Dou¹, Chao Qin¹, Mohan Dunga¹ (¹Sandisk Technologies Inc.)
- P-09** Avalanche Breakdown in IGBT Corners with VLD Termination: Quantitative 3D TCAD Investigation
Massimiliano Galvagno¹, Simone Dario Mariani², Paola Zuliani², Salvatore-Fabio Liotta³, Silvia Cannizzaro³, Gerardo Malavena¹, Christian Monzio Compagnoni¹, Alessandro Sottocornola Spinelli¹ (¹Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy, ²STMicroelectronics, via C. Olivetti 2, 20864 Agrate Brianza, Italy, ³STMicroelectronics, strad. Primosole 50, 95121 Catania, Italy)
- P-10** Physics-Informed Compact Modeling of Leakage and Breakdown in GaN-on-Si Devices
Ilya Rumyantsev¹, Jeff Steinfeldt², Nyles Cody¹, Shuyi Li¹, Daniel Connolly¹, Marek Hytha¹, Robert J Mears¹, Daniel Bailey³, Jonathan W Anderson³, Edwin Piner³ (¹Atomera Inc., ²Sandia National Lab., ³Texas State Univ.)
- P-11** SOI PeDMOS R_{ON} - BV_{OFF} tradeoff optimization through TCAD simulations
Joris Lacord¹, Ayoub Boutayeb², Dominique Golanski², Sylvain Joblot², Fabienne Ponthenier¹ (¹CEA-Leti, ²STMicroelectronics)
- P-12** Double-Gate LDMOS Transistors with Exceptional Figure-of-Merit Exceeding 700 kW/mm²
Elham Mashhadi¹, William Gerard Vandenberghe², Sara Ghazvini², Ali Saadat³, Hal Edwards⁴, Sujatha Sampath⁴, Daniel Pham⁴ (¹Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX 75080, USA, ²Department of Material Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080, USA, ³Department of Kilby Labs, Texas Instruments Inc., Richardson, TX 75080, USA, ⁴Department of Analog Technology Development, Texas Instruments Inc., Richardson, TX 75080, USA)
- P-13** Unified TCAD Simulation Framework for InGaAs/InP Single-Photon Avalanche Diodes
M. Saqlain Khan¹, Andreas Woerl¹, Frank Rutz¹ (¹Fraunhofer-Institute for Applied Solid State Physics IAF)
- P-14** Revisiting Random Dopant Fluctuation at Cryogenic Temperature: the Effect of Incomplete Ionization
Huawei Tang¹, Yu Wu¹, Junjie Hao¹, Shaofeng Yu¹ (¹Fudan Univ.)
- P-15** Hot Carriers and Self-Heating Effects in FD-SOI Devices at Cryogenic Temperatures
Bhargav Nallan Chakravartula¹, Ziyi Wang², Siddhant Gangwal¹, Katerina Raleva³, Dragica Vasileska¹, Michael Povolotskyi⁴ (¹Arizona State University, ²onsemi, ³University Ss Cyril and Methodius, ⁴Amentum Solutions)
- P-16** DFT Modeling of O₂-Driven Fragmentation and Islanding from MoS₂ Nanoworms
Suman Gora¹, Jay Singh¹, Medha Shukla¹, Arnab Datta¹ (¹Indian Institute of Technology (IIT) Roorkee)
- P-17** Modeling and Simulation of Exciton Dynamics in Transition Metal Dichalcogenides Heterostructures
Rohit Ramesh Nimje¹, Athira S¹, Vignesh S¹, Ashutosh Mahajan¹ (¹Centre for Nanotechnology Research, Vellore Institute of Technology, Vellore-632014, India.)
- P-18** Analytical SOT MRAM Modeling : From Deterministic to Fokker-Planck based Stochastic Switching
Trisha Bhowmik^{1,2}, Maxwell Gama Monteiro¹, Siddharth Rao¹, Yang Xiang¹, Jan Van Houdt^{1,2}, Kristiaan Temst^{1,2}, Fernando Garcia Redondo¹, Gouri Sankar Kar¹ (¹Indus., ²Univ.)
- P-19** Quasi-Bound State Tunneling in GaN Devices using 2D NEGF with Supercell Mode-Space Method
Heonseok Oh¹, Phil-Hun Ahn¹, Jooseok Kim¹, Mincheol Shin¹ (¹Korea Advanced Inst. of Sci. and Tech.)
- P-20** Semi-Classical Monte Carlo Simulation of Contact Geometry Effect on Source/Drain Junction Resistance in N-Type Si Fin and Nanosheet FETs
Uiho Lee¹, Jaeyeon Kim¹, Jiwon Chang¹ (¹Yonsei Univ.)
- P-21** Carrier Density Dependent Transport in Monolayer WS₂
Nils Vansteenvoort^{1,2}, Andrés Hidalgo², Gautam Gaddemane², Bart Sorée^{1,2}, Maarten L Van de Put² (¹Univ. KU Leuven, ²Inst. Imec)
- P-22** Lattice-Based Quantum Phonon Transport in FD-SOI Transistors
David Mai¹, Dirk Schulz¹ (¹TU Dortmund University)

- P-23** FE-NEGF for Cryogenic Thermal Management
Arnaud Lorin¹, Jing Li¹ (¹Univ. Grenoble Alpes, CEA, Leti)
- P-24** A Fokker-Planck Approach for Modeling Temperature-Dependent Two-Phase Switching Dynamics in Ferroelectrics
Wei Zhang¹, Leming Jiao¹, Jianze Wang¹, Xiao Gong¹, Xuanyao Fong¹ (¹National Univ. of Singapore)
- P-25** Multi-Stage Etch Recipe Inverse Design: Bridging Expert Behavioral Cloning and Reinforcement Learning
Jianming Guo¹, Mingqiang Geng¹, Zhengming Liu², Dianyu Qi¹, Dong Ni¹, Dawei Gao^{1,2} (¹Zhejiang Univ., ²Zhejiang ICsprout Semiconductor Co., Ltd.)
- P-26** Layer-by-layer oxidation of HfSe₂ and formation of clean van der Waals interfaces with 2D semiconductors: A first-principles molecular dynamics study
Joonho Park¹, Yong-Hoon Kim¹ (¹Korea Advanced Institute of Sci. and Tech.)
- P-27** Twisting in High Aspect Ratio Etching with Charging Effects as a Stochastic Mechanism
Taishi Ikeda¹, Hisashi Kotakemori¹, Satoshi Nakamura¹, Kenta Yashima¹, Takumi Ohmura¹, Yasuyuki Kayama¹, YunTae Lee², Yukihide Tsuji², Shinwook Yi², Moon-Hyun Cha², Jaehoon Jeong² (¹Samsung Japan Corp., ²Samsung Electronics Corp.)
- P-28** Impact of Surface Charging on Feature Profile Evolution in 3D NAND Pillar Etching
Siddharth Mohanty¹, Vatsal Thakor², Om Maheshwari¹, Nihar Ranjan Mohapatra¹ (¹Indian Inst. of Tech. Gandhinagar, India, ²Nirma Univ., India)
- P-29** Pulsed Bias Etching of Silicon Pillar Arrays: Experiment and Surface-Memory Simulation of Loading Control
Jianming Guo¹, Zhengming Liu², Mingqiang Geng¹, Kunrun Song², Huiyun Jiang^{1,2}, Dong Ni¹, Dawei Gao^{1,2} (¹Zhejiang Univ., ²Zhejiang ICsprout Semiconductor Co., Ltd.)
- P-30** Experiment-Based Modeling of Wafer-to-Wafer Bonding for 3D Integration
Hyuga Ishii¹, Takashi Shimura², Ryota Ogata¹, Hayato Kitagawa¹, Taisuke Yamamoto¹, Fumihiro Inoue¹ (¹YOKOHAMA National University, ²ESTECH Corp.)
- P-32** Multi-Phase-Field Modeling of Thin-Film Silicidation
Christophe Pixius¹, Ferdinand Schulz¹, Sanjukta Chowdhury¹, Eberhard Baer¹, Christopher Straub¹, Andreas Roskopf¹ (¹Fraunhofer IISB)
- P-33** SEMulator3D[®] Linking Deposition Process to Electrical Metrics-Accelerated WAT Learning
Xing Qin¹, Tristan Yang¹, Deyong Kong¹, Xiaoqiang Wan¹ (¹Lam Research Corp.)
- P-34** SPER-Driven Dislocation Nucleation and Uphill Diffusion Modeling for Advanced Semiconductor Processing
Chihak Ahn¹, Alexander Schmidt², Joohyun Jeon², Seungmin Lee², Woosung Choi¹, Jaehoon Jeong² (¹Samsung Semiconductor Inc., ²Samsung Electronics)
- P-35** Feature Charging During Cryogenic Plasma Etching
Yeon Geun Yook¹, Chenyao Huang¹, Yifan Gui¹, Mark J. Kushner¹ (¹Univ. of Michigan)
- P-36** A Covariance Matrix Adaptation Evolutionary Strategy Parameter Extractor for BSIM-CMG
Jen-Hao Chen¹, Ahtisham Pampori¹, Chenming Hu¹, Sayeef Salahuddin¹ (¹Univ. of California, Berkeley)
- P-38** Comprehensive SPICE Compact Modeling of Split-Gate Embedded Flash Memory for Transient and Worst-Case Operation Failure Simulation
Dongwoo Lim^{1,2}, Kiyoung Kim², Hyungcheol Shin¹ (¹Seoul National Univ., ²Samsung Electronics Co., Ltd.)
- P-39** SPICE Modeling Method of Reverse Recovery Based on TCAD Analysis
Emiru Baba¹, Shigeru Nakajima¹, Tsuyoshi Kachi¹, Takuma Hara¹, Kozo Kinoshita¹ (¹Toshiba Electronic Devices & Storage Corporation)
- P-40** First-principles calculation of free carrier absorption in 4H-SiC
Masahiko Matsubara¹, Enrico Bellotti¹ (¹Boston University)
- P-41** Low-temperature enhancement of quantum hybridization-induced negative differential resistance in a Pb-free 1D halide perovskite
Jeongwon Lee¹, Tae Hyung Kim¹, Juho Lee¹, Yong-Hoon Kim¹ (¹Korea Advanced Inst. of Sci. and Tech.)
- P-42** Multi-space density functional simulations of WSe₂ p-n junctions
Hyeonjun Kang¹, Taehyung Kim¹, Juho Lee¹, Ryonggyu Lee¹, Yonghoon Kim¹ (¹Korea Advanced Inst. of Sci. and Tech. (KAIST))

- P-43** Machine Learning Framework for the Inverse Design of Tight-Binding Parameters in Compound Semiconductors
Kaito Seike¹, Shingo Sato¹ (¹Kansai University)
- P-44** A Machine-Learning Accelerated Atom-to-Transistor Simulation Framework
Pratik Brahma¹, Krishna Bhattaram¹, Sayeef Salahuddin¹ (¹University of California, Berkeley)
- P-45** Physics-Enhanced LSTM Modeling of Electric Double-Layer Transistors
Haoran Yang^{1,2}, Shuaidi Zhang^{1,2}, Yue Zhao^{1,2}, Ling Li^{1,2} (¹Inst. of Microelectronics, CAS, ²Univ. of CAS)
- P-46** Power-Performance Assessment of 48 nm Gate-Pitch CFETs Using Experimentally Calibrated Physics-Informed ANN Models
Yu-Wen Xu¹, Yiming Li¹, Min-Hui Chuang¹, Yun Tai¹ (¹National Yang Ming Chiao Tung Univ.)
- P-47** AI-driven TCAD Surrogate Modeling and Multi-Objective Optimization for Accelerated Technology Development
Derek Dou¹, Sudarshan Narayanan¹, Qinghua Zhao¹, Chao Qin¹, Mohan Dunga¹ (¹Sandisk Tech., Inc.)
- P-48** Accelerating Simulation of General Gate-All-Around Transistors via a Quasi-1D Model
Gyubeen Kim¹, Kwang-Woon Lee², Sung-Min Hong² (¹Department of Semiconductor Eng., Gwangju Inst. of Sci. and Tech., ²Department of Electrical Eng. and Computer Sci., Gwangju Inst. of Sci. and Tech.)
- P-49** Machine Learning Accelerated Geometry Optimization under External Electric Fields
Yuanchen Chu¹, Guido Gandus¹, Kantawong Vuttivorakulchai², Marton Voeroes¹, Hong-Hyun Park¹, MinYong Jeong², Mohammad Ali Pourghaderi², Uihui Kwon², Yoon-Suk Kim², Seungmin Lee², Woosung Choi¹, Jaehoon Jeong² (¹TCAD lab, Samsung Semiconductor Inc., San Jose, CA, United States, ²Computational Science and Engineering Team, Samsung Electronics, Yongin-si, Gyeonggi-do, Republic of Korea)

Wednesday, September 30, 2026 (Kumamoto-Jo Hall)

Session 9: Advanced CMOS Devices (Room A1, 3F)

- Chairpersons: Mitsuhiro Sengoku (Toshiba)
Masaru Miyashita (Rapidus)
- 9-01** 9:00 - 9:30 **[invited talk]**
Efficient DC Simulation of Monolithic CFETs Using a Quasi-1D Approach
Sung-Min Hong¹ (¹Gwangju Institute of Science and Technology)
- 9-02** 9:30 - 9:50
Impact of 4F2 DRAM Access Transistor Design on Floating Body Effect and Retention
Ashish Pal¹, Lars P. Tatum¹, Rohit Gupta¹, El Mehdi Bazizi¹, Subi Kengeri¹ (¹Applied Materials)
- 9-03** 9:50 - 10:10
Multiscale Modeling of Channel Surface Roughness: Impact on Front-End-of-Line And Circuit Performance for Advanced Logic Technology
Ning Yang¹, Pratik B. Vyas¹, Rohit Gupta¹, Ashish Pal¹, El Mehdi Bazizi¹, Subi Kengeri¹ (¹Applied Materials Inc.)
10:10 - 10:30 Coffee Break (Exhibition Area, Foyer, 3F)
- 9-04** 10:30 - 10:50
Impact of Thermal Expansion Mismatch-Induced NMOS Metal Gate Stress on MBCFET Performance
Sung-Ho Kim¹, Sooyoung Park¹, Chang Ju Moon¹, Jong Su Kim¹, Jaehong Lee¹, Yoon-Suk Kim¹, Seung Hyun Song¹, Yonghee Park¹, Jaehoon Jeong¹ (¹Samsung Electronics Corp., Ltd.)
- 9-05** 10:50 - 11:10
Modeling of Soft Errors in CFET SRAM Using Machine Learning-Assisted Circuit Simulation
Vanness Filbert Cierra¹, Yoshinari Kamakura¹ (¹Osaka Inst. Tech.)
- 9-06** 11:10 - 11:30
Low-Temperature Behavior in Silicon Nanowire n-FETs Studied by Atomistic NEGF
Sanam Moslemi-Tabrizi², Peter Schvan², Philippe Blaise¹, Udit Kapoor¹, Daniel Lemus³, Tillmann Kubis³ (¹Silvaco Inc., ²Ciena Inc., ³Purdue Univ.)

Session 10: Defects, Reliability and Variability (Room A2, 3F)

Chairpersons: Jaehyun Lee (Pusan National Univ.)
Yuki Ohuchi (Fuji Electric)

- 10-01** 9:10 - 9:30
Multi-Scale Statistical Modeling of Random Telegraph Noise in Sub-Micrometer CIS
Jae Ho Kim¹, Sungchul Kim¹, Yonghee Park¹, Jonhyun Go¹, Jae Hoon Jung¹ (¹Samsung Electronics)
- 10-02** 9:30 - 9:50
Antisite Disorder in the Native Oxide Insulator β -Bi₂SeO₅: A First-Principles Study
Mina Bahrami Bahrami¹, Mohammad Rasool Davoudi¹, Dominic Waldhoer¹, Christoph Wilhelmer¹, Pedram Khakbaz¹, Theresia Knobloch¹, Michael Waltl¹, Tibor Grasser¹ (¹Institute for Microelectronics)
- 9:50 - 10:30 Coffee Break (Exhibition Area, Foyer, 3F)
- 10-04** 10:30 - 10:50
Modeling the Memory Window Distribution in FeFETs Considering Grain Variability
Kenichiro Sonoda¹, Shibun Tsuda¹, Tadashi Yamaguchi¹, Atsushi Amo¹, Eiji Tsukuda¹ (¹Renesas Electronics Corp.)
- 10-05** 10:50 - 11:10
Modeling Counterclockwise Current Hysteresis in Oxide Thin-Film Transistors
Pranay Baikadi¹, Benius Dunn¹, Javier Meza-Arroyo¹, Sara Ghazvini¹, Julia W. P. Hsu¹, William G. H. Vandenberghe¹ (¹University of Texas at Dallas)
- 10-06** 11:10 - 11:30
Disentangling Hysteresis in Emerging Transistors: Beyond Threshold Shifts to Area-Based Decomposition
Mohammad Rasool Davoudi¹, Dominic Waldhoer¹, Mina Bahrami¹, Alexander Karl¹, Pedram Khakbaz¹, Axel Verdianu¹, Michael Waltl¹, Theresia Knobloch¹, Tibor Grasser¹ (¹TU Wien (Technische Universität Wien))
- 10-07** 11:30 - 11:50
First-Principles Evaluation of *p*-type Conductivity in Zn-Doped Bismuth Oxyselenide (Bi₂O₂Se)
Christoph Wilhelmer¹, Tibor Grasser¹ (¹TU Wien)
- 11:30 - 13:00 Lunch Break (Room A3+A4, 3F)

Session 11: Artificial Intelligence and Machine Learning (Room A1, 3F)

Chairpersons: François Triozon (CEA-Leti)
Lado Filipovic (TU Vienna)

- 11-01** 13:00 - 13:20
Atomistic Modeling of Mg-Ion Implantation into GaN using an Efficient Machine-Learned Interatomic Potential
Yuki Ohuchi^{1,3}, Robert Stella^{2,3}, Sabine Leroy^{2,3}, Lado Filipovic^{2,3} (¹Advanced Technology Laboratory, Fuji Electric Corp. Ltd., ²CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors at the, ³Inst. for Microelectronics, TU Wien)
- 11-02** 13:20 - 13:40
k-space resolved surrogate models for efficient inverse design of optical metasurfaces
Damien Maitre^{1,2}, Francesco Guadagnuolo¹, Jean-Philippe Banon², Maxime Darnon², Raphaël Clerc², Loumi Tremas¹, Mathys Le Grand¹, Adam Fuchs¹, Pascal Urard¹, Coumba Gaye¹, Olivier Jeannin¹, James Downing¹, Denis Rideau¹ (¹STMicroelectronics 2. Univ. Jean Monnet, CNRS, Institut d'Optique Graduate School, Laboratoire Hubert Curien UMR 5516)
- 11-03** 13:40 - 14:00
Physics-Informed Neural Networks for Stable Drift-Diffusion Simulation and Inverse Parameter Extraction in 2D Semiconductors Devices
Satofumi Souma¹, Akiko Ueda² (¹Kobe Univ., ²AIST)

11-04 14:00 - 14:20

A Deep Learning Framework for Fast, Unified Process and Device TCAD Simulation

Konstantina Kovani¹, Greta Chiaravalli¹, Francesco Di Stefano¹, Michal Dyrek¹, Semin Kwak¹, Vamsi Spandan Arza¹, Ryota Hachiya², Yonggwi Cho², Hideki Minari², Jun Komachi², Shinya Yamakawa², Lorenzo Servadei¹ (¹AI for Chip Design Team, Sony AI, Sony Europe, Zurich, Switzerland, ²Sony Semiconductor Solutions Corp., Tokyo, Japan)

Session 12: Thermal Transport and Electro-Thermal Modeling (Room A2, 3F)

Chairpersons: Junichi Hattori (AIST)
Nobuhiko Nakano (Keio Univ.)

12-01 13:00 - 13:20

A Novel 2.5D Thermal Coupling Model for Device/Metal Reliability Applications

Jyun-Yan Kuo¹, Gary Lee¹, Kasa Huang¹, Jeffrey Tzeng¹, Y.S. Lin¹, S.H. Li¹, Y.L. Chang¹, H.P. Chien¹, P.C. Hsu¹, G.T. Lin¹, W.C. Chang¹, Eugene Chen¹, C. C. Lai¹, Tony Yu¹, M.H. Hsieh¹, Clement Huang¹, K.Y. Su¹, Jim Liang¹, K.W. Su¹, C.K. Lin¹ (¹Taiwan Semiconductor Manufac. Company)

12-02 13:20 - 13:40

Joule heating and thermal transport in 2D materials for device applications

Zlatan Aksamija¹, Sylvester Makumi¹, Aidan Belanger¹ (¹Univ. of Utah)

12-03 13:40 - 14:00

Monte Carlo Modeling of Phonon Drag Effects on Thermoelectric Transport in Silicon Nanostructures with doping modulation

Jerome Saint-Martin^{1,2}, Mohammad Ghanem¹, Raja Sen³, Jelena Sjakste³, Philippe Dollfus¹ (¹Université Paris-Saclay, CNRS, Centre de Nanosciences et de Nanotechnologies, ²Université Paris-Saclay, ENS Paris-Saclay, CNRS, SATIE, ³Laboratoire des Solides Irradiés, CEA-DRF-IRAMIS, École Polytechnique)

Closing (Room A1, 3F)

14:30 - 14:45 **Closing Remarks**

Hideki Minari (Sony Semiconductor Solutions Corp.)